

Release 2022 R1 Highlights

Signal & Power Integrity

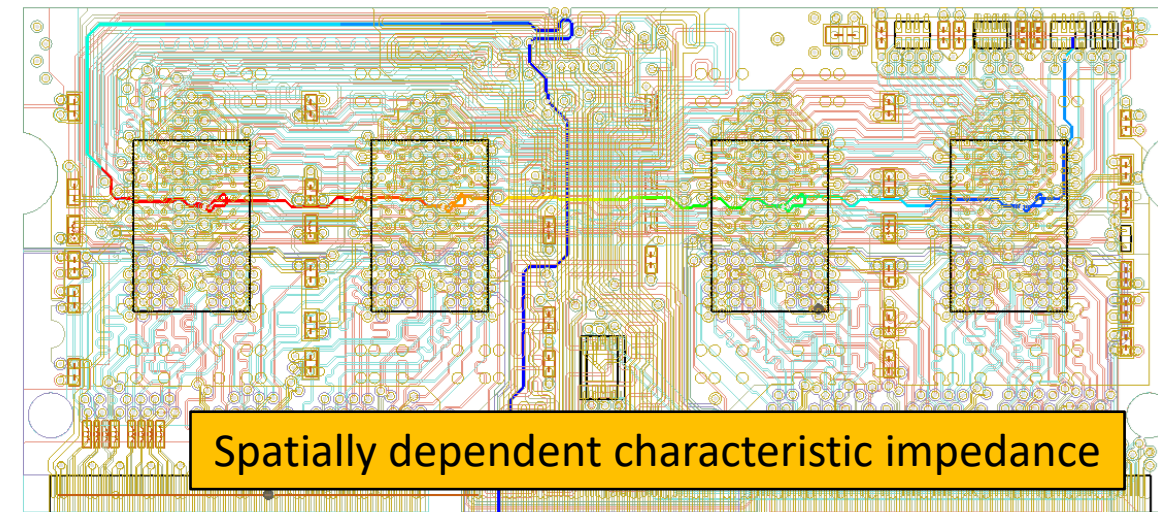
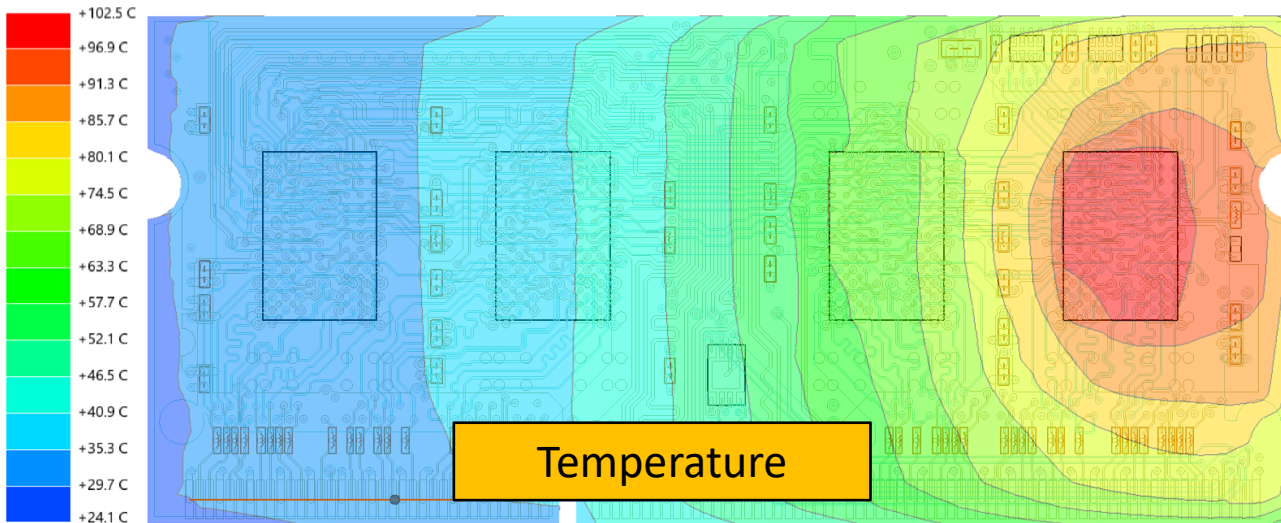
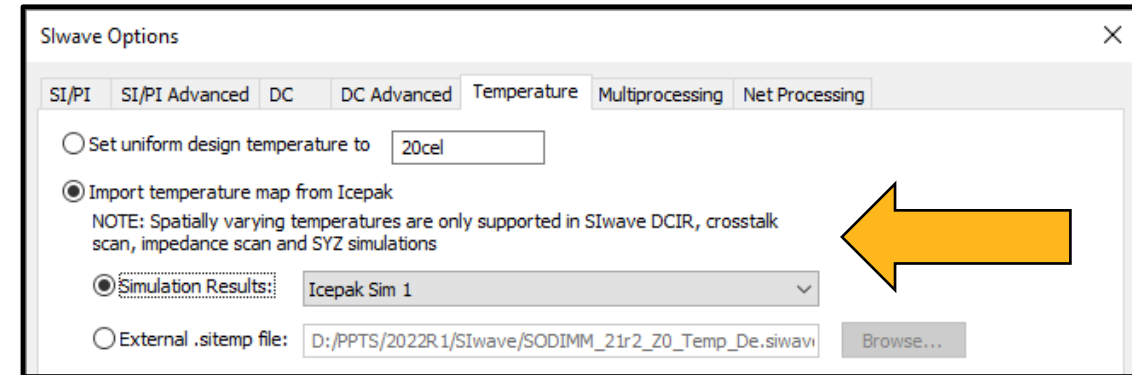


SIwave

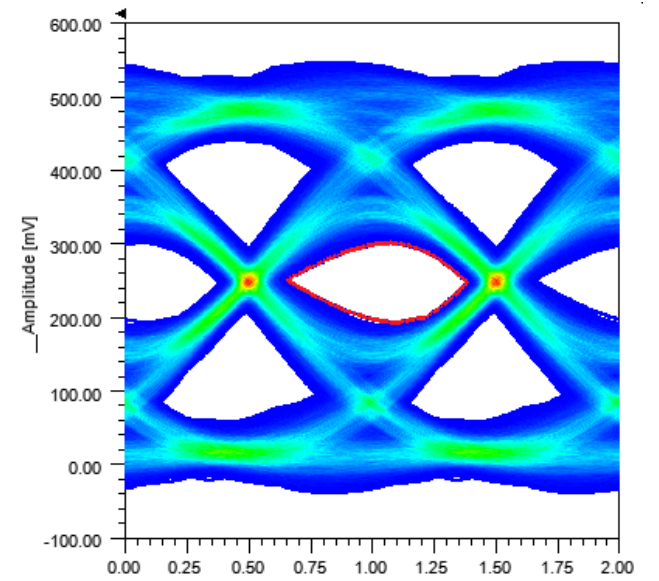
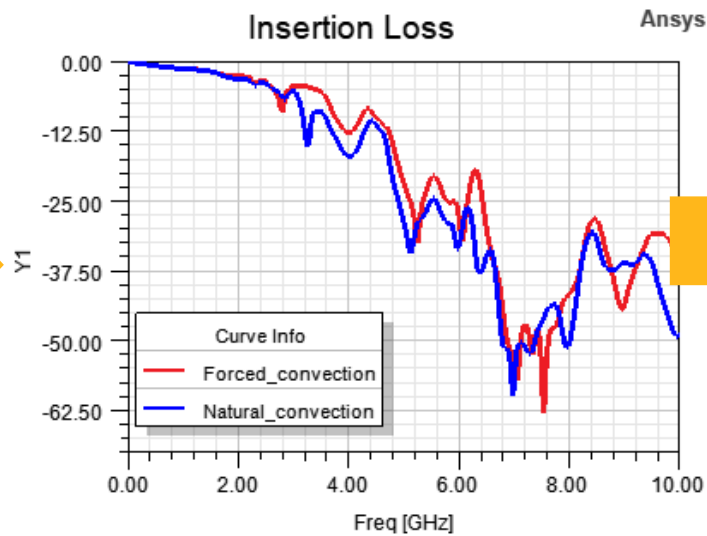
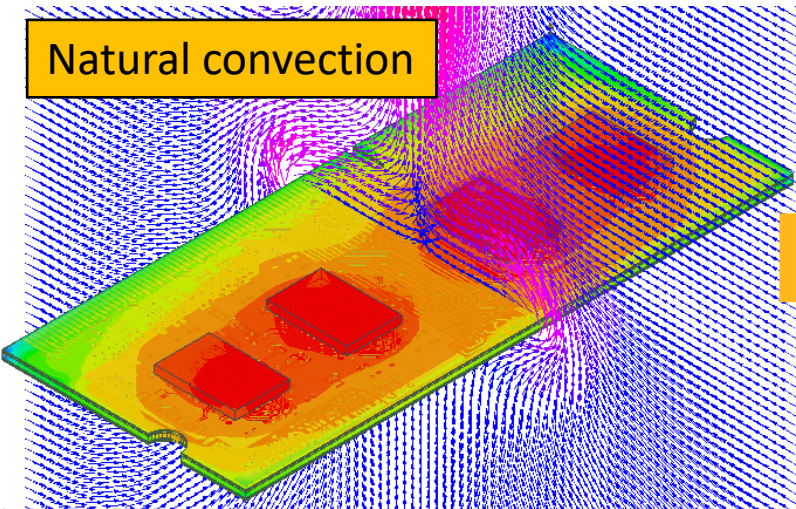
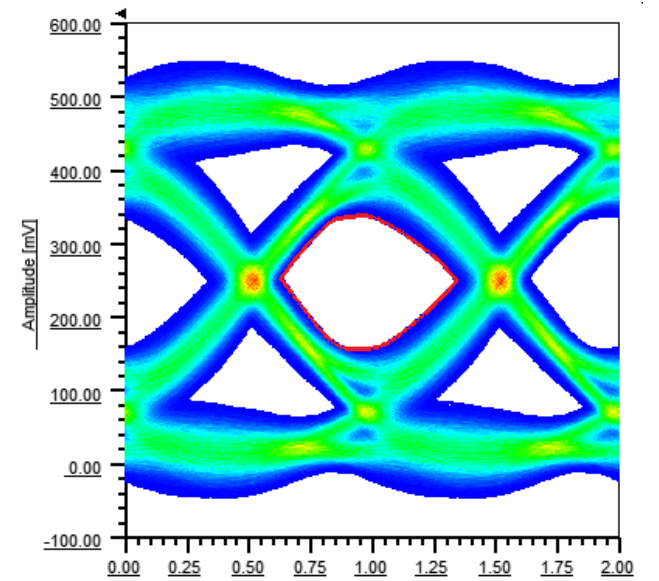
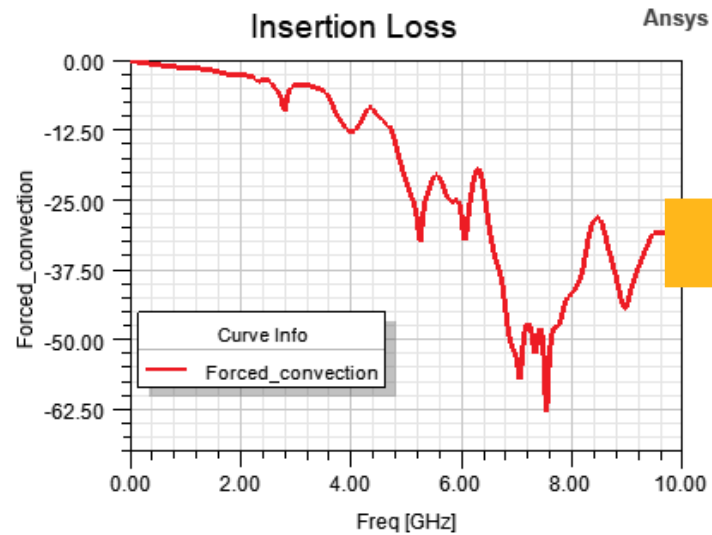
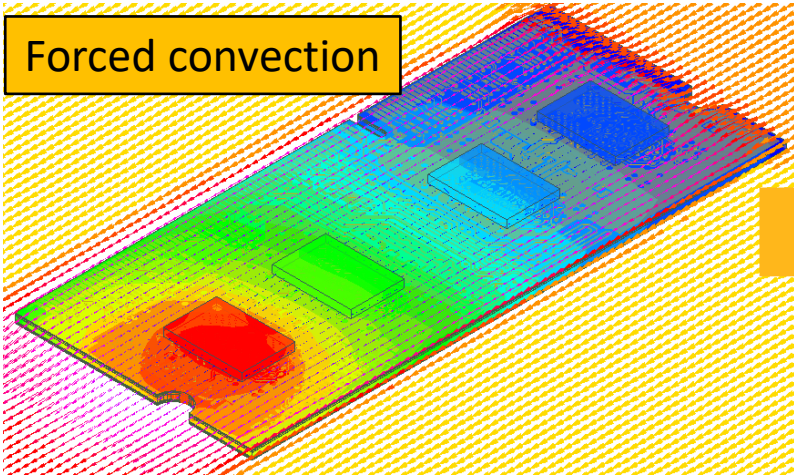
ANSYS

Temperature dependent materials in Siwave AC

- Temperature map import from Icepak
- Thermal modifier applied to dielectric materials and conductors
- Non-uniform temperature distribution supported
- Spatially dependent permittivity and conductivity for plane (FEM) and trace (MoM) models



Temperature dependent materials in SIwave AC



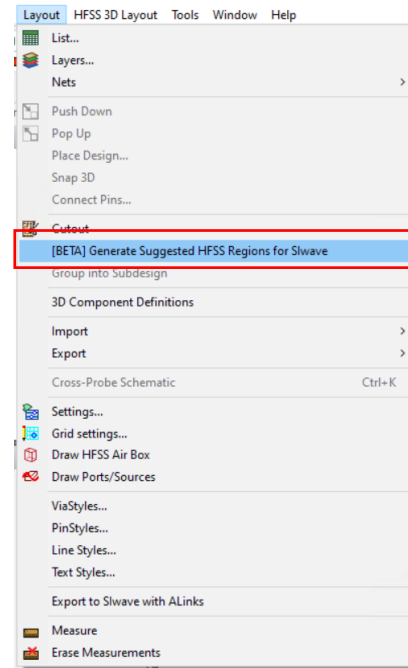
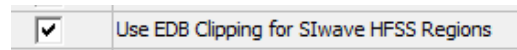
SIwave HFSS Regions

[BETA] Auto (suggested) SIwave HFSS Regions in 3D Layout

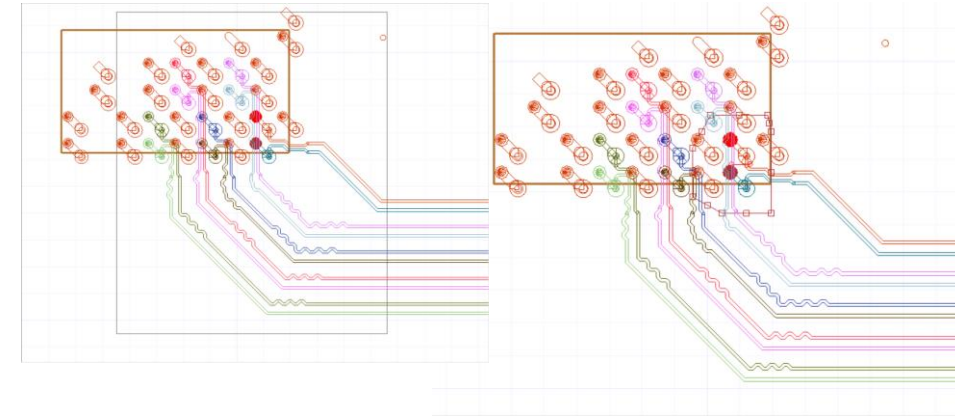
- Creates HFSS Regions around areas of significant 3D activity
- Guarantees Electrical Coherence for HFSS Simulations
- Regions are a suggestion; users can modify or remove regions they dislike

[BETA] EDB-based Region Clipping

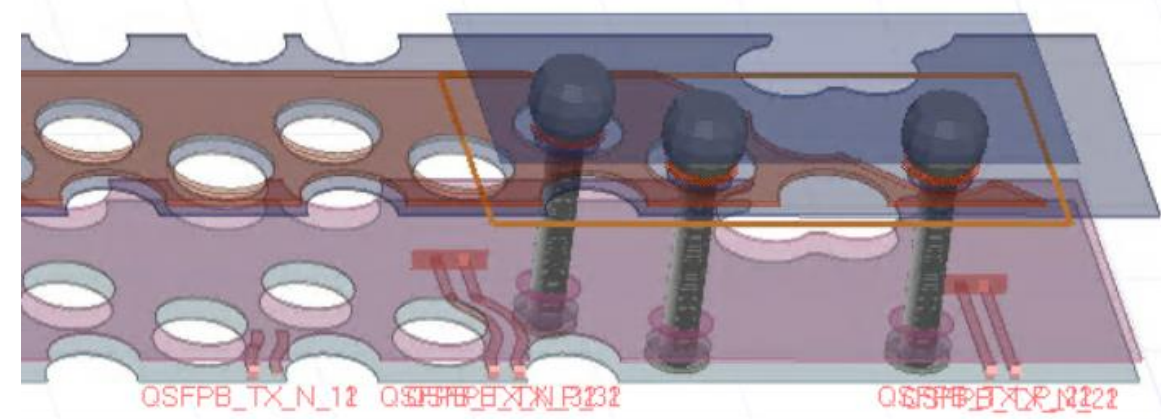
- When launched from 3D Layout, replaces ClipDesign during preparation HFSS Regions
- Operates directly on an EDB, preserving EDB-only elements such as waveports
- Activate through Beta Feature



User-Defined HFSS Region Auto HFSS Region



Waveports in an SIwave HFSS Region



SIwave HFSS Regions

Ansys Electronics Desktop 2021 R2 - siwave_1 - siwave_1 - Layout - [siwave_1 - siwave_1 - Layout]

File Edit View Project Draw Layout HFSS 3D Layout Tools Window Help

Save Cut Undo Copy Paste X Delete siwave_1 top Zoom Pan Rotate Fit All Fit Selected

Unite Duplicate Flip Subtract Convert Rotate Intersect Reverse Line Align Cutout Healing Geometry Check

Half Grid VRMs HFSS Extents XY Plane Pin Groups List 90deg Workflow Layout Settings

Desktop View Layout Simulation Results Automation Ansys Minerva

Project M... siwave_1*

Properties

Message Manager Progress

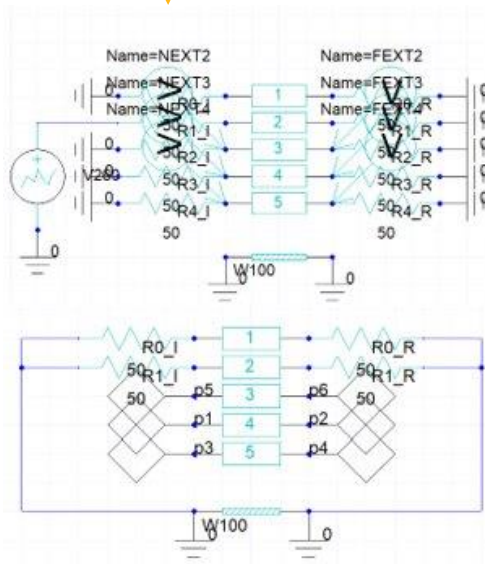
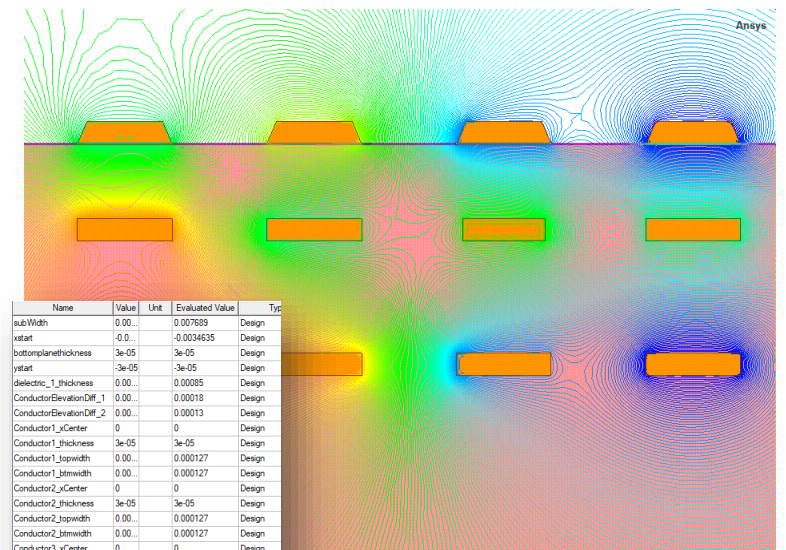
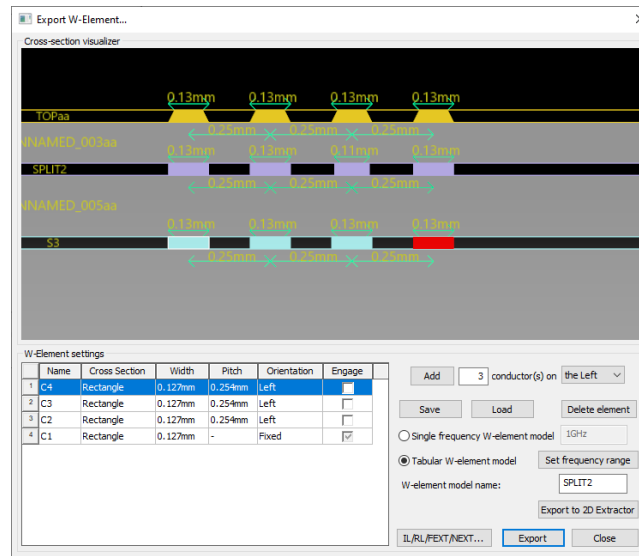
Ready Hide 0 Messages Hide Progress X: Y: Delta X: Delta Y: Distance: cm Angle:

The screenshot displays the Ansys SIwave HFSS Regions interface. The central workspace shows a PCB layout with various components and traces. The traces are color-coded by net, with green and blue being prominent. The right side of the interface features several panels:

- Classification:** A dropdown menu set to '<All>', with '<Power/Ground>' selected below it.
- Nets:** A list of nets including GND, GPIO0 through GPIO11, P3.3V, TX_HDMI_5V, TX0_TMDS0_N, TX0_TMDS0_P, TX0_TMDS1_N, TX0_TMDS1_P, TX0_TMDS2_N, TX0_TMDS2_P, TX0_TMDS3_N, TX0_TMDS3_P, and USBIN_N.
- Layers:** A panel with checkboxes for 'Show Dielectrics', 'top', 'bottom', 'Measures', 'Outline', 'SIwave Regions', 'Rats', 'Errors', 'Symbols', and 'Postprocessing'. The 'SIwave Regions' checkbox is checked.

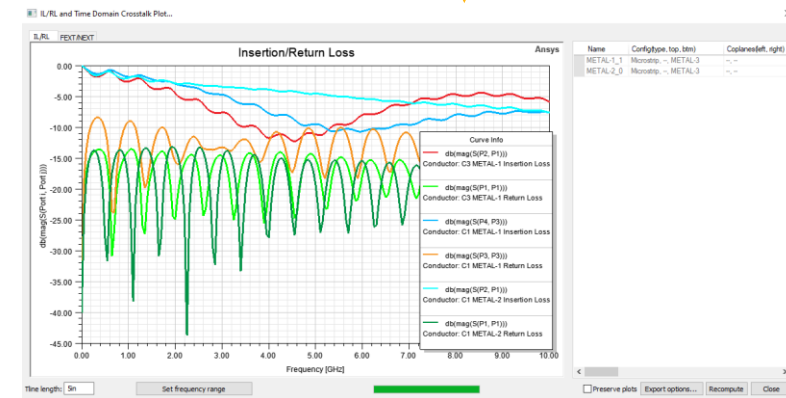
Stackup Wizard

- Ability to define/engage multiple conductors in one simulation
 - Multiple ports for linear network analysis
 - Multiple victims for cross talk analysis
- Engage multiple conductors across selected layers
- Fully parameterized 2D extractor export
 - Conductor pitch/width/thickness/etch
 - Conformal, dielectric, signal layer thickness and elevation
- Circuit schematic and Touchstone file export supports multi-layer conductor models
- Supported in W-element cross section analysis feature in Siwave and 3D layout
- Available in Siwave, 3D Layout, SIXplorer



```
.model METAL_2 W MODELTYPE=table N=5 RMODEL=r_METAL_2 LMODEL=l_METAL_2
+ GMODEL=g_METAL_2 CMODEL=c_METAL_2

.model r_METAL_2 sp N=5 SPACING=nonuniform VALTYPE=real INTERPOLATION=spline
+ DATA = 201
+ 0
+ 4.055073744176896
+ 0.1762478313507305
+ 4.055073096384399
+ 0.17624801623092
+ 0.1762476907538527
+ 4.055073739311627
+ 0.1762476849395631
+ 0.1762474980415142
+ 0.176247816390236
+ 4.05507308330342
+ 0.1762473012408656
+ 0.1762472512887582
+ 0.1762475649231423
+ 0.1762474198571742
+ 4.055072960333503
+ 5.0001e+07
+ 12.52327914475038
+ 3.917965670496883
+ 12.28708487733427
+ 1.643272494940398
+ 1.927034379780823
+ 12.45151741432435
+ 1.94341064668603
+ 2.383207896174993
+ 3.916533155247656
+ 12.43124791478647
+ 0.3927632631888349
+ 0.6403262907800001
+ 1.862729893995752
+ 2.1762478313507305
```



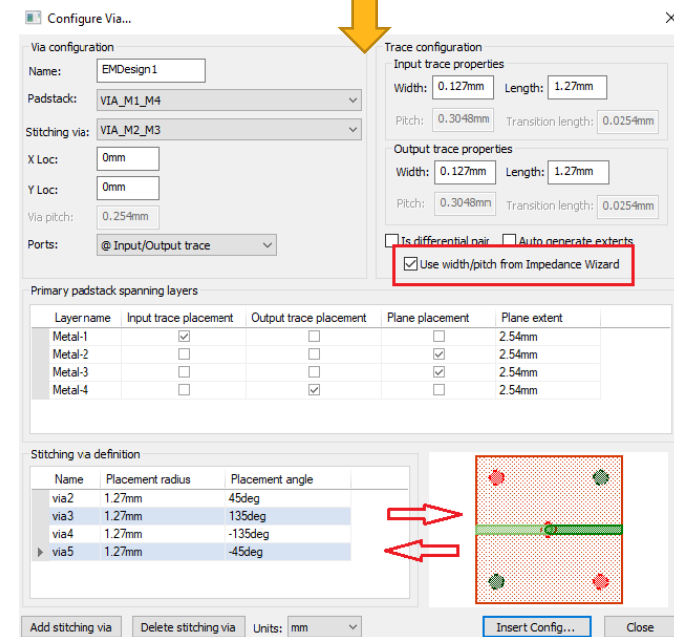
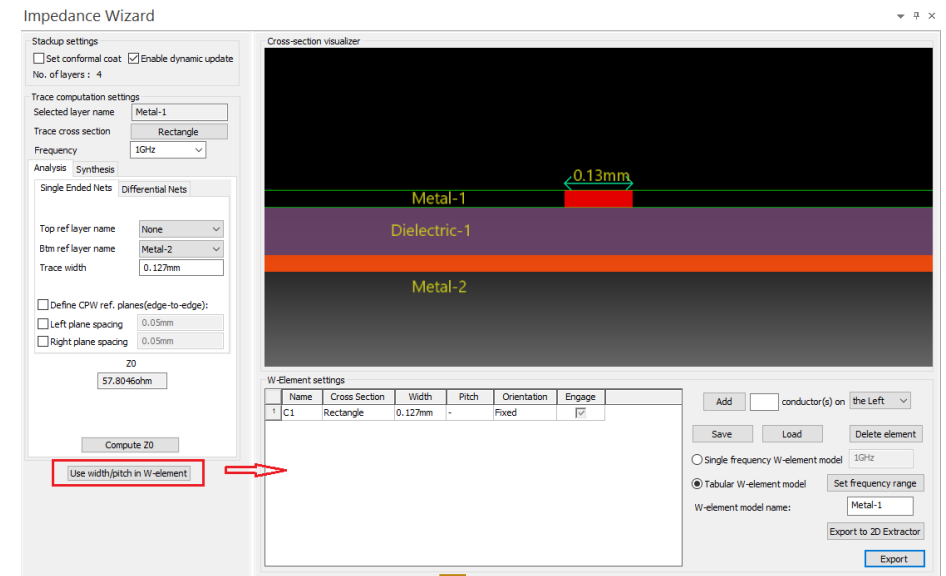
SIXplorer

Via Wizard

- Freeform stitching via placement
 - Stitching via location is defined using placement radius and angle
 - Support copy/paste of entire grid row to add new definition
 - Allow bulk updates to values of placement radius and angle by clicking on corresponding column header
- Addition of 2D top-down EDB preview in via configuration dialog
 - Two-way selection between grid row and 2D view
- Propagate synthesized/analyzed trace width/pitch from Impedance wizard to Via wizard
- Allow import of stackup and padstacks from unsourced/non-SIXplorer AEDT projects/EDBs

Impedance Wizard

- Ability to save/restore UI state at application close/launch



EMI Scanner

- Rule-checking Improvements
 - Use more appropriate distance metrics in various rules
 - Proper handling of curved traces
- Edge-to-edge vs center-to-center
- Distribution of vias over grid rather than just simple count
- Additional details and images in exported reports

- New Rule: Disparate Reference Overlap
 - Requested for CMOS image sensor development
- Power supply noise sensitive to coupling of digital reference and analog reference
 - Define a set of nets whose planes cannot overlap with planes from the other set
 - Violations issued if total overlap area exceeds a threshold

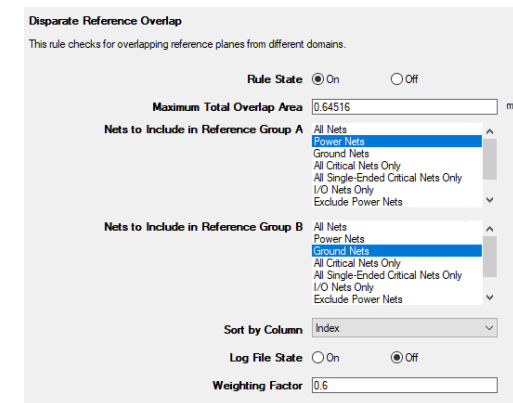
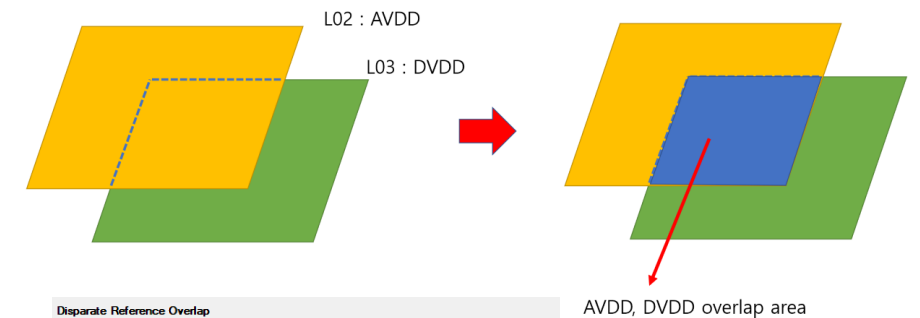
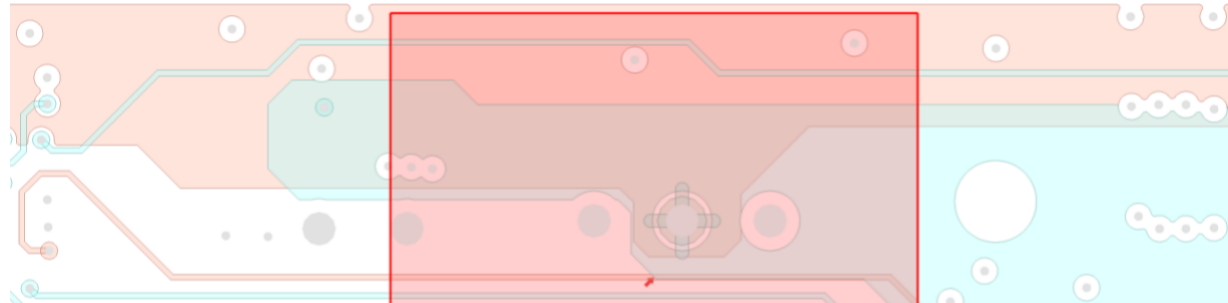
EMI Violations

Rule Type: Signal Reference

Rule Name: Critical Net Crossing Split Reference Plane

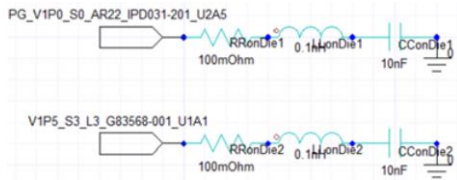
Rule Description: Critical nets must not cross a split in the adjacent reference plane. Notes: 1. Any crossing of an adjacent plane by a critical net will cause a violation. 2. A crossing is allowed if two stitching capacitors (one on either side of the crossing point) are within a specified distance of the crossing.

Violation 1: Cap Search Box = [(23.622, 51.1302) | (38.862, 66.3702)], Gap Point = (31.242, 58.7502), Net = A0_GPIO, Reference Layer = LVR_1, Signal Layer = LVR_2

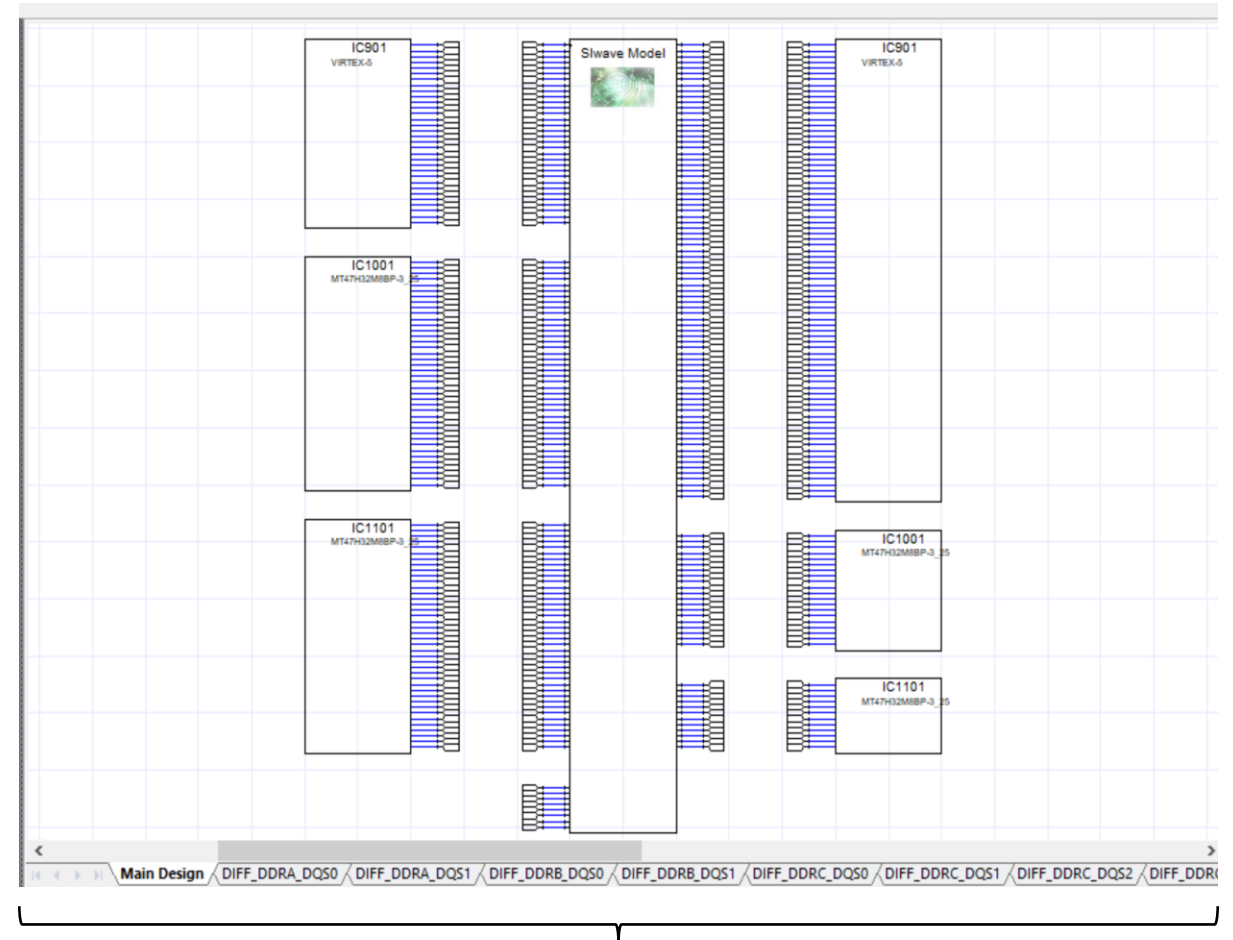
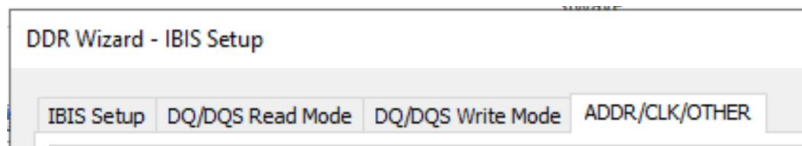


DDRwizard

- Schematic organized in multiple tabs
- Main tab contains dynamic-link block along with driver/receiver components
- Nets grouped by byte lanes with corresponding strobe
- Separate tab for IBIS blocks
- OnDie RLC support for VRM nets



- New tab for ADDR/CLK/OTHER nets in IBIS assignment dialog

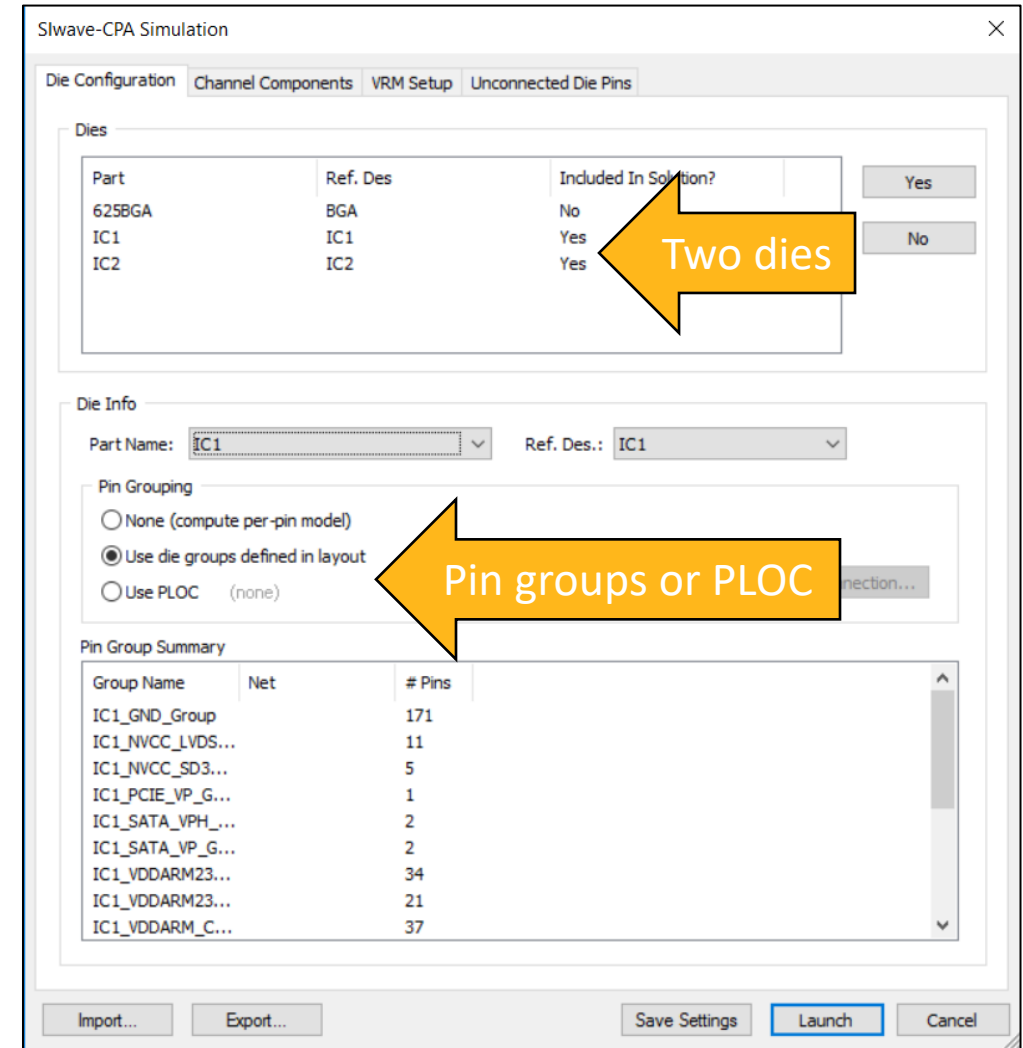
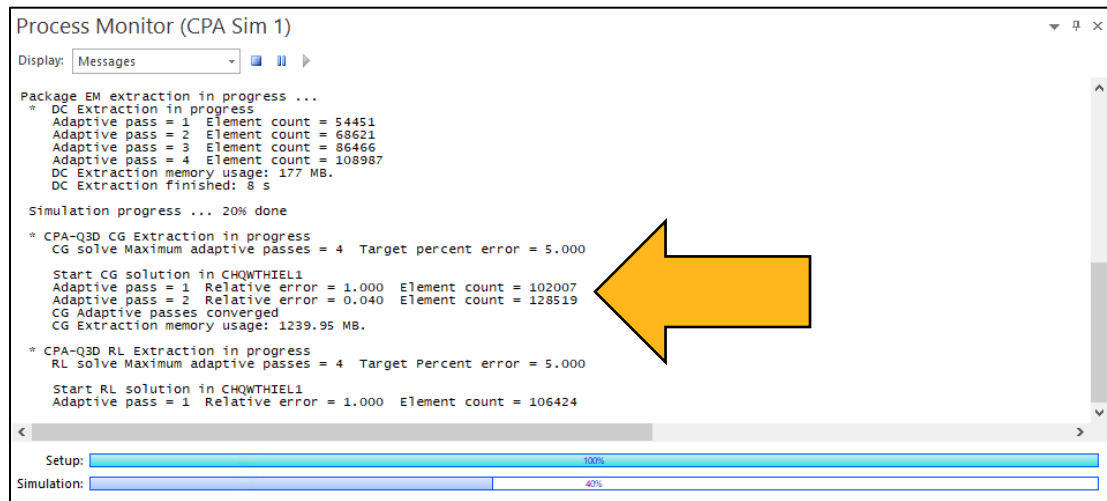


DDR schematic organized into logical tabs

CPA Solver

- Multi-Die and Multi-PLOC support
 - Extract RLCG for multiple dies
 - Import and connect PLOC/CPM or set the Pin Grouping model for each die individually
- Adaptive process update and messaging in real time for CPA-Q3D solver

```
Process Monitor (CPA Sim 1)
Display: Messages
Package EM extraction in progress ...
* DC Extraction in progress
  Adaptive pass = 1 Element count = 54451
  Adaptive pass = 2 Element count = 68621
  Adaptive pass = 3 Element count = 86466
  Adaptive pass = 4 Element count = 108987
  DC Extraction memory usage: 177 MB.
  DC Extraction finished: 8 s
Simulation progress ... 20% done
* CPA-Q3D CG Extraction in progress
  CG solve Maximum adaptive passes = 4 Target percent error = 5.000
  Start CG solution in CHQWTHIEL1
  Adaptive pass = 1 Relative error = 1.000 Element count = 102007
  Adaptive pass = 2 Relative error = 0.040 Element count = 128519
  CG Adaptive passes converged
  CG Extraction memory usage: 1239.95 MB.
* CPA-Q3D RL Extraction in progress
  RL solve Maximum adaptive passes = 4 Target Percent error = 5.000
  Start RL solution in CHQWTHIEL1
  Adaptive pass = 1 Relative error = 1.000 Element count = 106424
```



Slwave-CPA Simulation

Die Configuration Channel Components VRM Setup Unconnected Die Pins

Part	Ref. Des	Included In Solution?	Yes	No
625BGA	BGA	No		
IC1	IC1	Yes		
IC2	IC2	Yes		

Two dies

Die Info

Part Name: IC1 Ref. Des.: IC1

Pin Grouping

None (compute per-pin model)

Use die groups defined in layout

Use PLOC (none)

Pin Group Summary

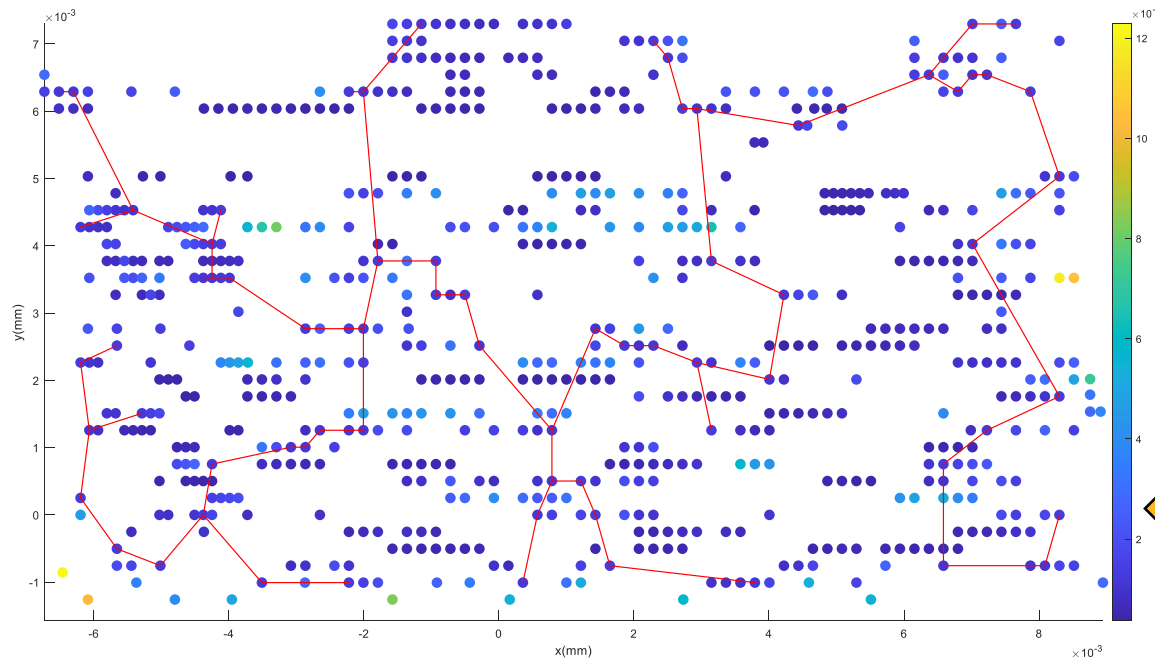
Group Name	Net	# Pins
IC1_GND_Group		171
IC1_NVCC_LVDS...		11
IC1_NVCC_SD3...		5
IC1_PCIE_VP_G...		1
IC1_SATA_VPH_...		2
IC1_SATA_VP_G...		2
IC1_VDDARM23...		34
IC1_VDDARM23...		21
IC1_VDDARM_C...		37

Pin groups or PLOC

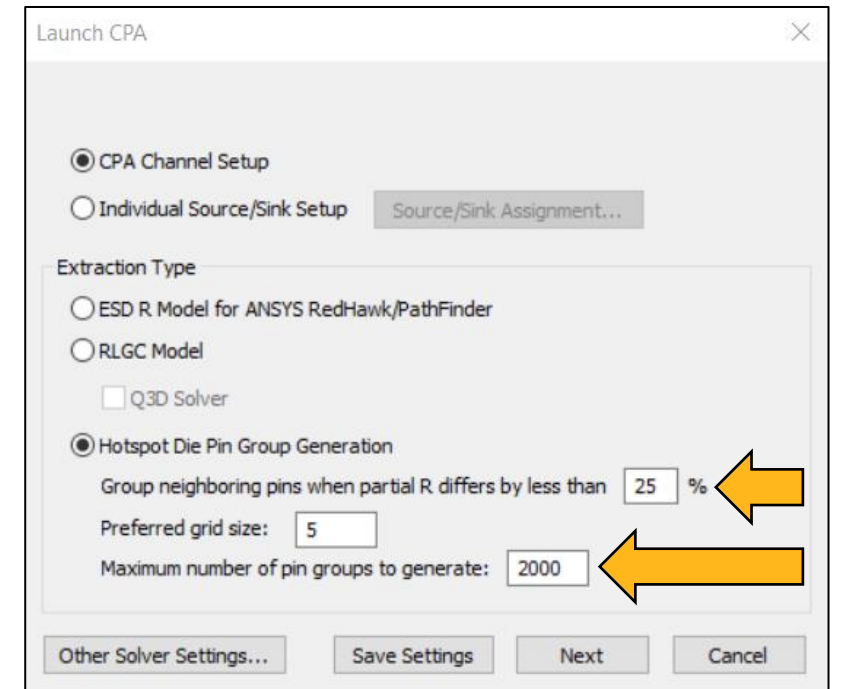
Import... Export... Save Settings Launch Cancel

CPA Solver

- Smart pin group enhancements
 - Cluster-based pin grouping algorithm with user-specified percentage (ΔR) maximum pin group number



One connected pin group on colormap



- PLOC to smart pin group matching
 - Apply hotspot pin groups to die components by preserving the PLOC connectivity data

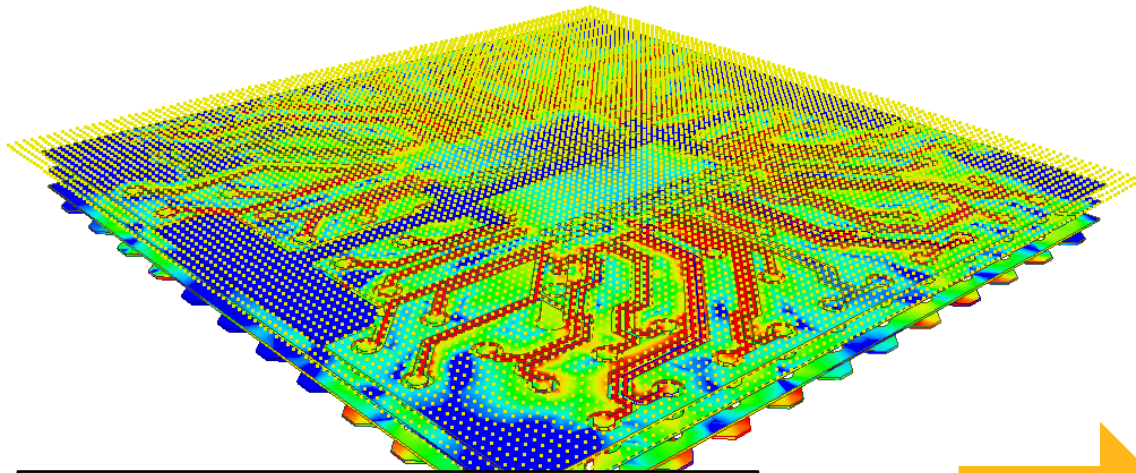
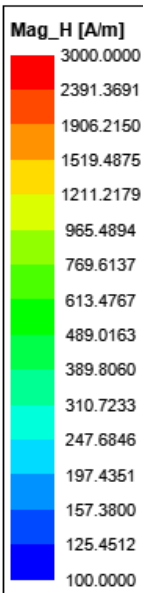
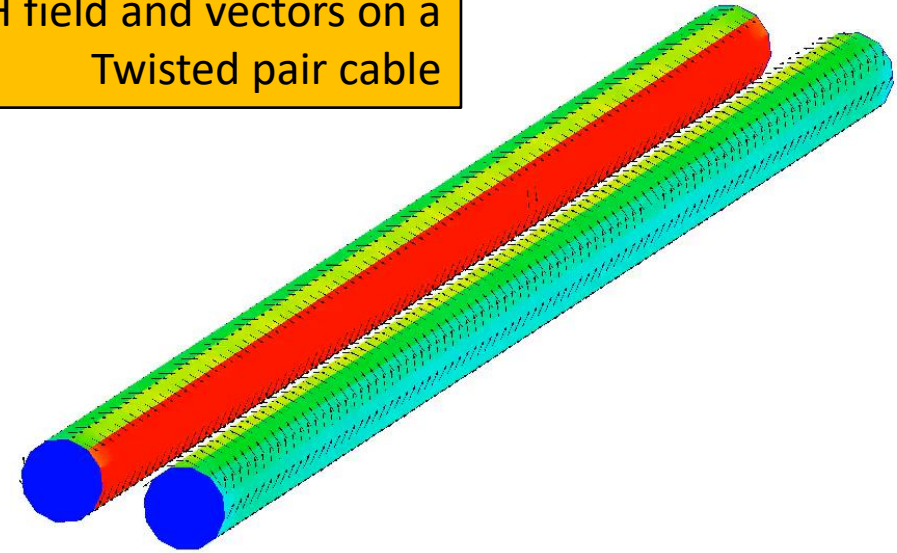
Q3D Extractor



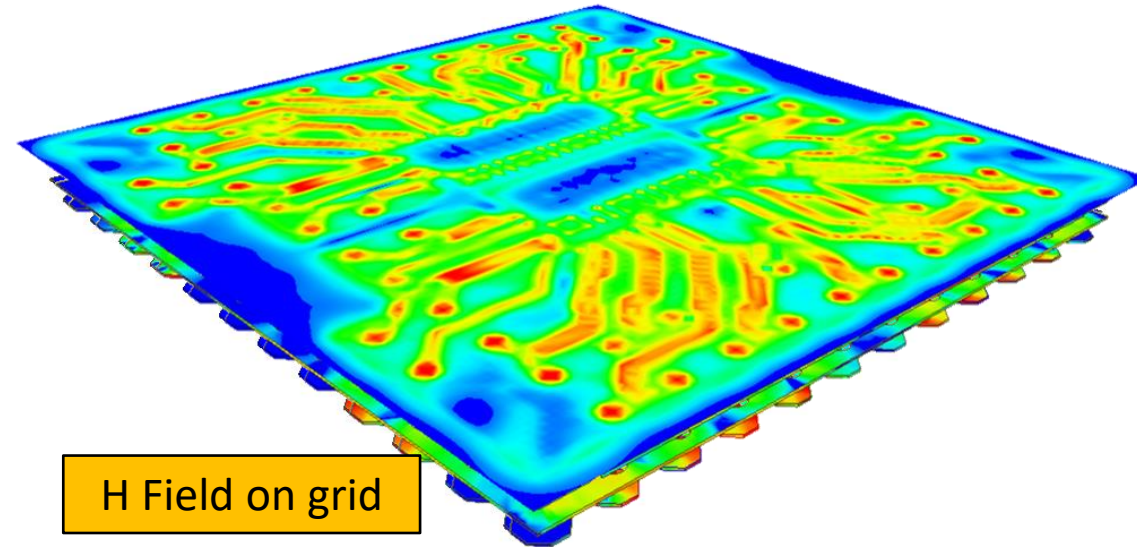
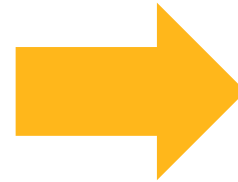
Magnetic field visualization for AC-RL

- Support H field overlay and export to Enight
- Support H field report on user defined EM fields setup
 - Box, Line, Rectangle, Sphere
- 2D contour plot overlay to modeler window

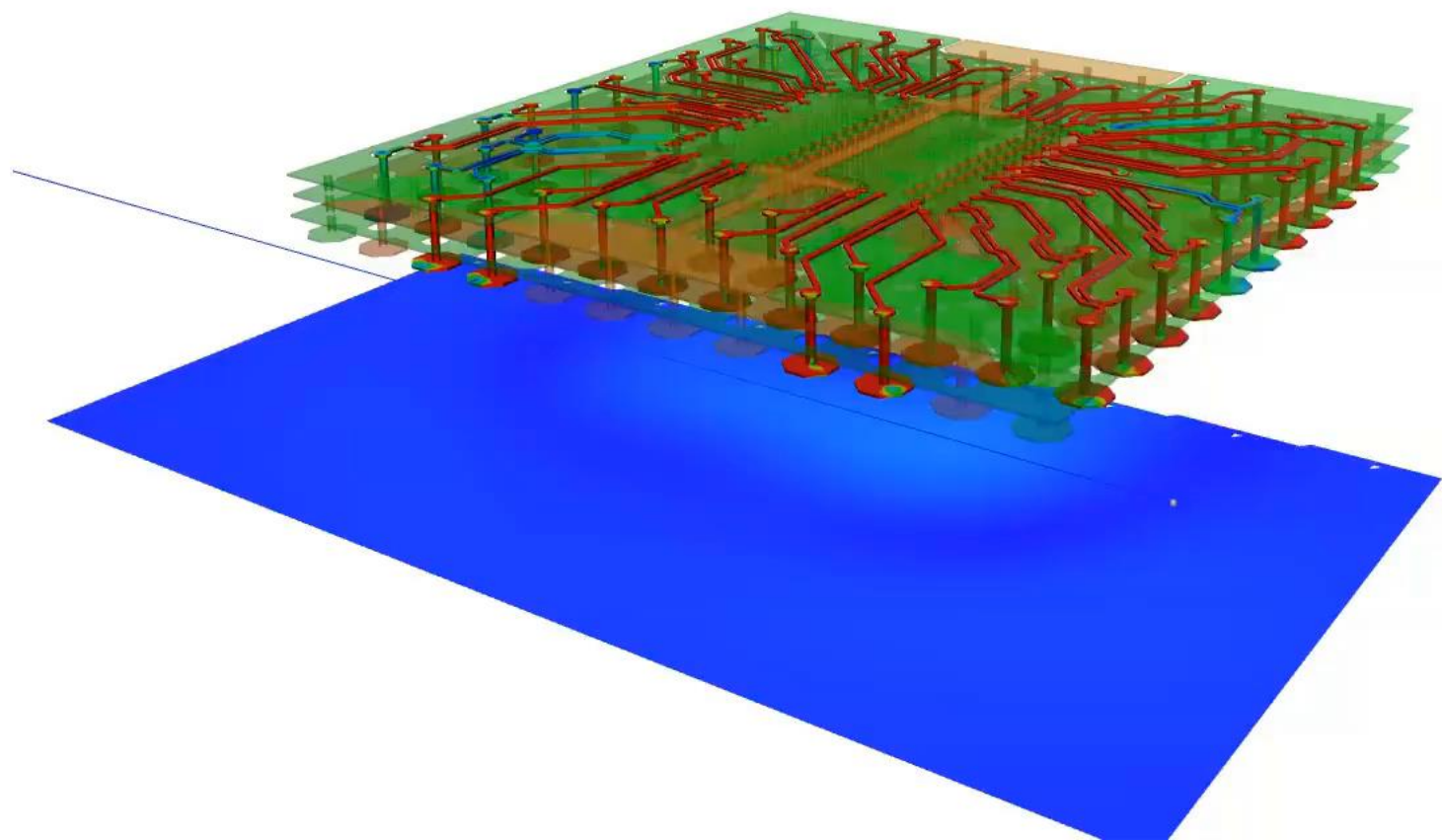
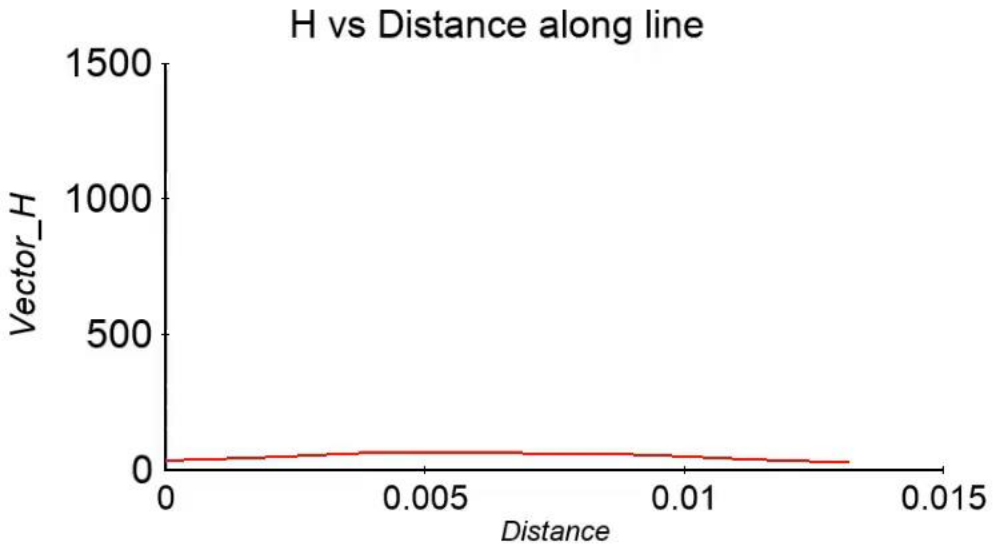
H field and vectors on a Twisted pair cable



Rectangular grid 1mm over package

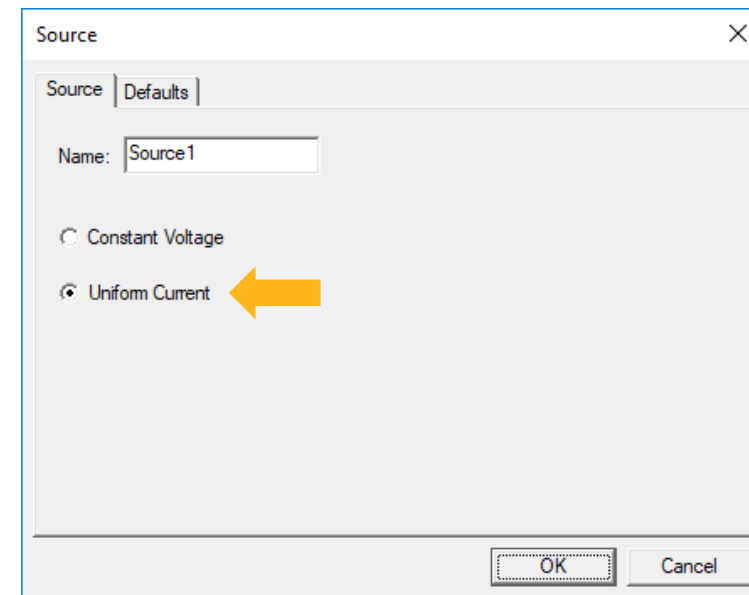
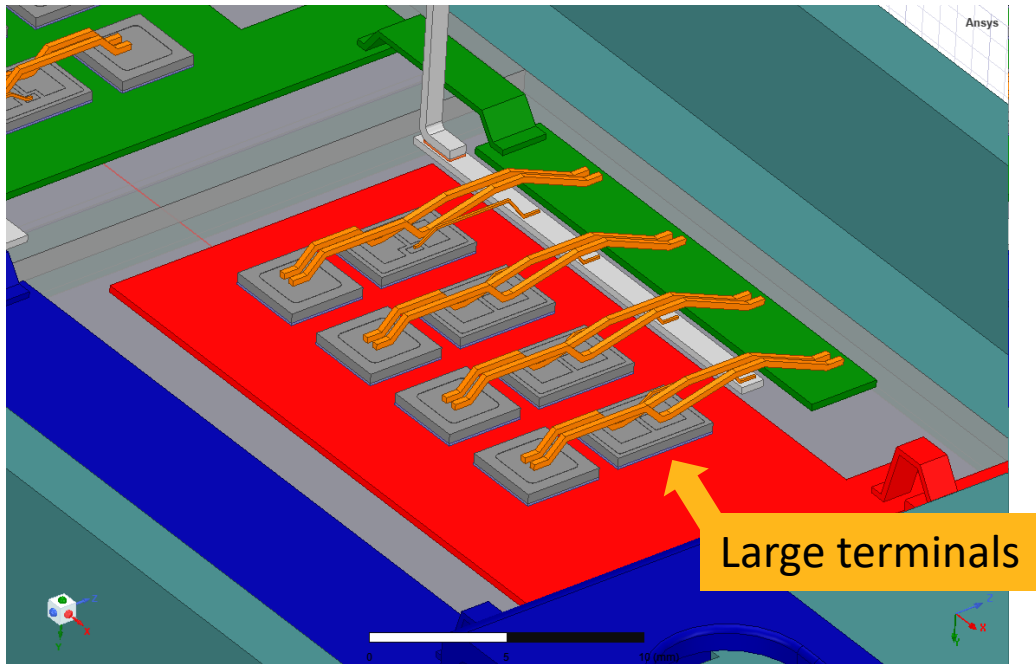


H Field on grid



Uniform current terminals for AC-RL and DC-RL

- Released uniform current terminals for the DC-RL solver
 - Uniform current and constant voltage terminals can coexist
 - Required for modeling power modules
 - Adding additional terminals will not impact the inductance

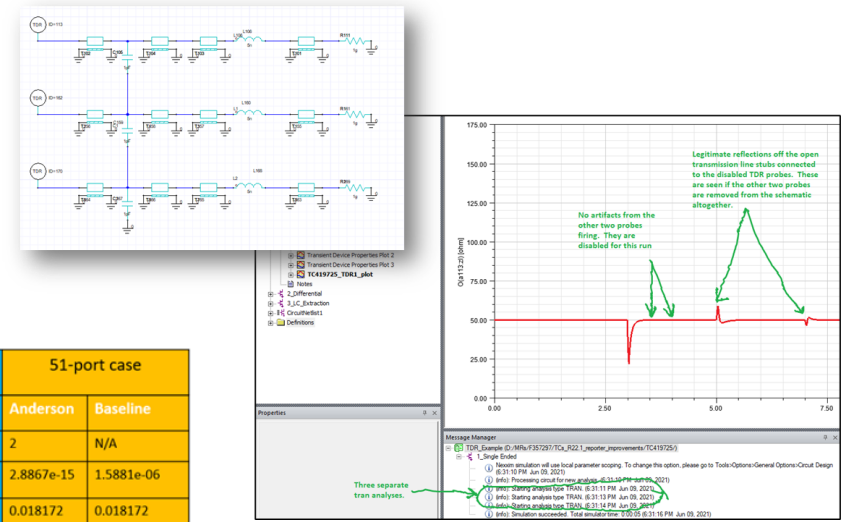


Circuit

Ansys

Circuit

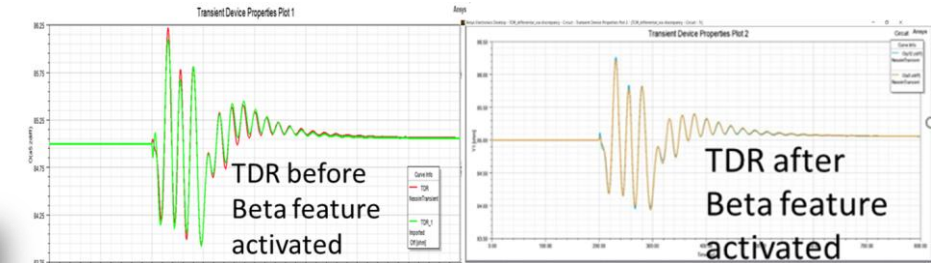
- Multiple TDR Probes
 - Improved behavior of Circuit when multiple TDR probes are used.
 - Provides better accuracy for coupled channels.
- Passive DC Fit Enhancement for “IFPVLF”
 - Enforce passivity sometimes destroys the fit at low frequency/DC.
 - The new “IFPVLF” DC passivity enhancement with Anderson Acceleration improves the DC passive fit of “IFPVLF”.
 - Now (R22.1) a full feature in both Nexxim and NDE including N-port and Dynamic Link (DL)



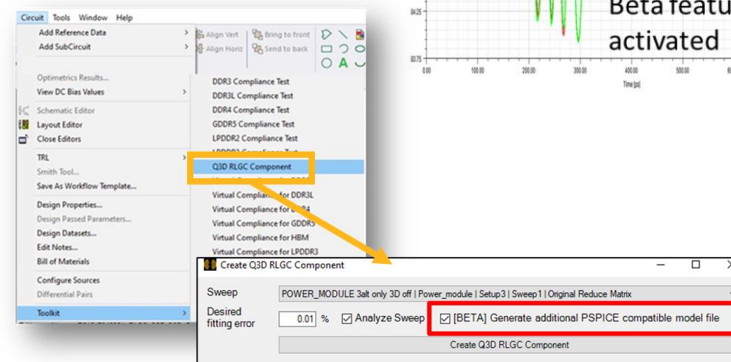
	6-port case		32-port case		51-port case	
	Anderson	Baseline	Anderson	Baseline	Anderson	Baseline
Iterations	17	N/A	2	N/A	2	N/A
DC error	5.0016e-10	0.003	3.2637e-10	6.6921e-09	2.8867e-15	1.5881e-06
Fitting error	0.23949	0.23961	0.0050348	0.0050348	0.018172	0.018172

IFPV -- Iterated Fitting of Passivity Violations (default)
 IFPVLF -- Do IFPV with passivity enforcement of DC/Low Frequency fit to “Z”

- Dynamic Link Frequency Sampling Points for Circuit-Field Solver CoSim [Beta]
 - Previously, the exact sweep, discrete or interpolating, S-data calculated by the field solver was not used by Circuit - Circuit chose its own set of discrete 501 uniform samples between DC and maximum.
 - This 22.1 beta feature ensures that the user specified sweep S-data is being passed to Circuit for state-space fitting.



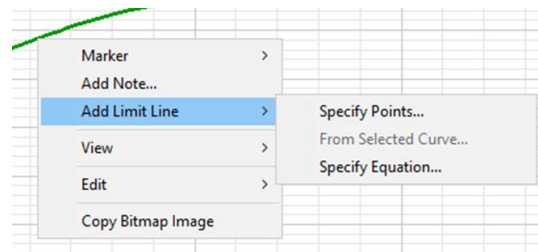
- PSPICE Model Export for Q3D RLGC State-Space Fitting [Beta]
 - “Q3D RLGC Component” Circuit toolkit introduced at 2021 R2.
 - Creates Circuit component based on state-space fitting of Q3D RLGC data for improved accuracy in many power electronics applications.
 - The toolkit can now export a PSPICE-compatible model file.



Network Data Explorer

- NDE Scripting [Beta]
 - Added script commands to oNDE = oDesktop.GetTool("ndExplorer")
 - Postprocessing: renormalization, deembedding, differential pairs
 - Transforms: all supported SPsim transforms, Smoothing, Termination
 - HasSameData function to compare data from two NetworkData objects
 - Documentation is in place
 - Released as Beta because some commands may change in the future

- Limit Lines
 - Associated with a particular network data and matrix entry, e.g. S11
 - Persistent until the network data is closed or AEDT closes



Circuit Scripting Guide

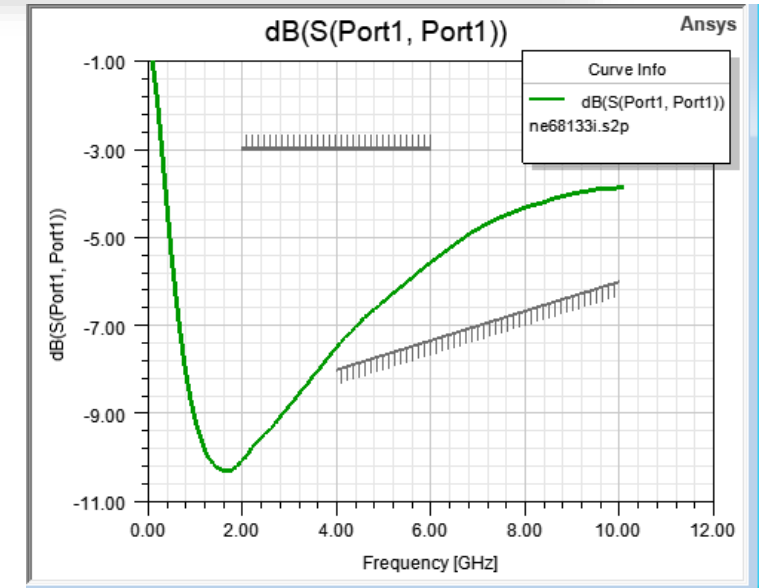
Network Data Explorer Script Commands

Network Data Explorer (NDE) scripting uses three objects, each with unique script commands:

- **Network Data Explorer** – top-level object obtained by calling `oNDE=oDesktop.GetTool("ndExplorer")`. network data Explorer commands are called using `oNDE`.
- **Network Data** – single set of S-parameters, corresponding to a single entry in the UI tree. Network Data commands are called using `oData`.
- **Post Process Settings** – settings that can be applied and removed from network data without making permanent changes to the underlying data. Post Process Settings commands are called using `oPostProc`.

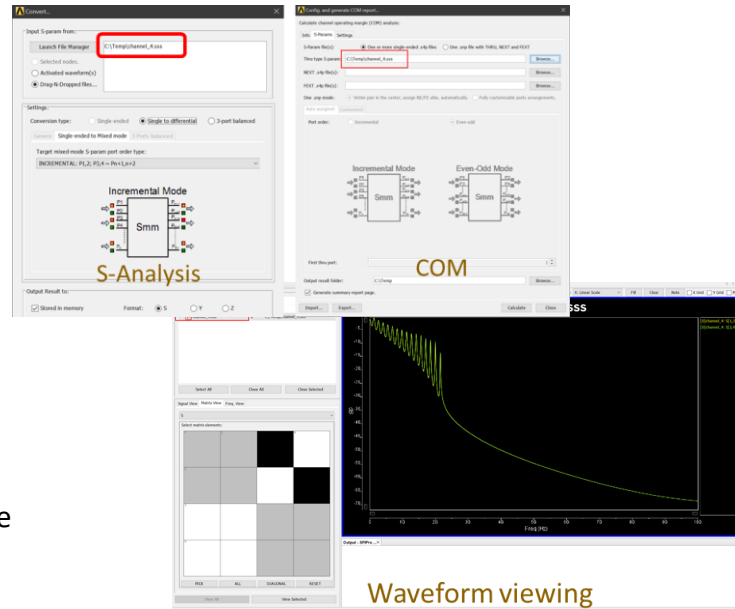
Examples using the above objects:

```
oNDE = oDesktop.GetTool("ndExplorer")
oData = oNDE.Open("D:\folder\test.s2p")
success = oPostProc.AddDiffPair(2, 1, "Diff1", "Comm1", 100, 25)
```



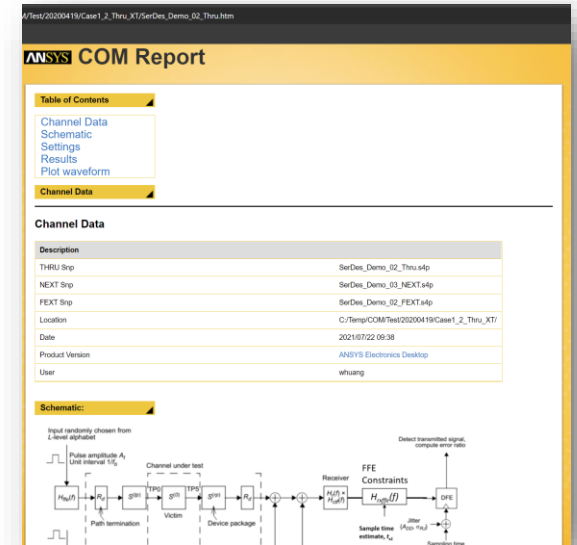
- State Space Model Support

- .sss reading is now supported in all of SPISim's viewer/s-param infrastructure.
- SPISim's waveform and all S-param related analysis, including COM, can now take .sss file as input for processing.



- Expose SPISim COM Outputs in AEDT [BETA]

- Support COM directly via AEDT's toolkit:
 - Generate summarized reports with all settings, results and plots in one place/page.
 - Also includes a waveform viewer for exploring interactively.
- Allows users to utilize SPISim's COM analysis capabilities much more directly with integrated look & feel and reports.



- Run COM in non-gui (NG) batch mode

- Customized flow and analysis
- Optimization (iterative)

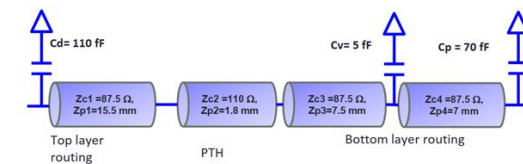
```
C:\Program Files\AnsysEM\V221\Win64\spisim\spisim\modules\ext>SPISimJNI_WIN64.exe COM -v CFGFILE=C:/Temp/COM/Test/20200419/Case1_2_Thru_XT/RestERL_cfg
[INFO]: Executing SPISimJNI in NON-GUI mode...
[ParmDat]: COM=-5.6351 -6.7771,ILD=0.5317 0.5317,ICN=3.9362 3.9362,ERL=18.5110 18.5110
```

- SPISim COM implementation updated to reference ver. V2.57

- COM can now support 802.3cd and 802.3ck specs.

- Flexible Package Model added

• http://www.ieee802.org/3/ck/public/18_09/mellitz_3ck_01_0918.pdf



Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.0404e-3 4.201e-4]	
package_tl_tau	6.325E-03	ns/mm
package_Z_c	[87.5 87.5 ; 110 110; 87.5 87.5; 87.5 87.5]	Ohm [1x Rx]

C_d	[1.e-4 1.1e-4]
z_p select	1
z_p [TX]	[15.5 20 30; 1.8 0.0; 7.5 0.0; 7.0 0.0]
z_p [NEXT]	[15.5 20 30; 1.8 0.0; 7.5 0.0; 7.0 0.0]
z_p [FEXT]	[15.5 20 30; 1.8 0.0; 7.5 0.0; 7.0 0.0]
z_p [RX]	[15.5 20 30; 1.8 0.0; 7.5 0.0; 7.0 0.0]
C_p	[0.7e-4 0.7e-4]
C_v	[5e-6 5e-6]

IEEE 802.3 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force

HFSS 3D Layout

Ansys

IC and GDS Workflow

- Geometric/simplification functions
 - **Add “convert to circle”** (UI and XML)
 - **Critical-net based hole removal in GDS processing** (XML)
 - Support metal layer union (UI and XML)
- Workflow and setup automation
 - Preview stackup from GDS import dialog
 - Import ports from csv file in GDS import dialog
 - Net tracing display/improvements in GDS import dialog
 - **Enable port referencing to closest pin on a net** (XML)
 - **Improve pin creation based on points** (XML)
 - **Improve auto-component creation** (XML)
 - Support relative path for component models (XML)
 - Use polygons on layer to create seeding-by-region operation (XML)
 - Create shapes on metal layer (XML)
- Modeling features
 - Solve-inside by region
 - **Add TSV option to via layer** (UI and XML)

Primary

Display: Stackup layers Non-stackup layers All layers

Stackup: Type: Units:

Name	Type	Material	Dielectric Constant	Thickness	Etch	Rough	Solver	Lower	Upper	Evaluated Lower	Evaluated Upper	Transparency
SB	signal	copper	1	35um				107.325um	142.325um	107.325um	142.325um	60
TOP	signal	copper	1	1.45um				105.875um	107.325um	105.875um	107.325um	60
V4	via	copper	1	0.775um				METAL3	TOP	105.1um	105.875um	60
METAL3	signal	copper	1	0.85um				104.25um	105.1um	104.25um	105.1um	60
V3	via	copper	1	0.85um				METAL2	METAL3	103.4um	104.25um	60
METAL2	signal	copper	1	0.85um				102.55um	103.4um	102.55um	103.4um	60
V2	via	copper	1	0.85um				METAL1	METAL2	101.7um	102.55um	60
DIEL	dielectric	silicon_dioxide	3.7	41.475um				0.10085mm	0.142325mm	0.10085mm	0.142325mm	60
METAL1	signal	copper	1	0.85um				100.85um	101.7um	100.85um	101.7um	60
V1	via	copper	1	100um				BOTTOM	METAL1	0.85um	100.85um	60
substrate	dielectric	silicon	12	100.85um				0mm	0.10085mm	0mm	0.10085mm	60
BOTTOM	signal	copper	1	0.85um				0um	0.85um	0um	0.85um	60

Layer

Insert above...
Insert below...
Remove
Select all

Edit selected

Name: V1
Type: via
Material: copper
Thickness: 100um
Top bottom: neither

Visibility

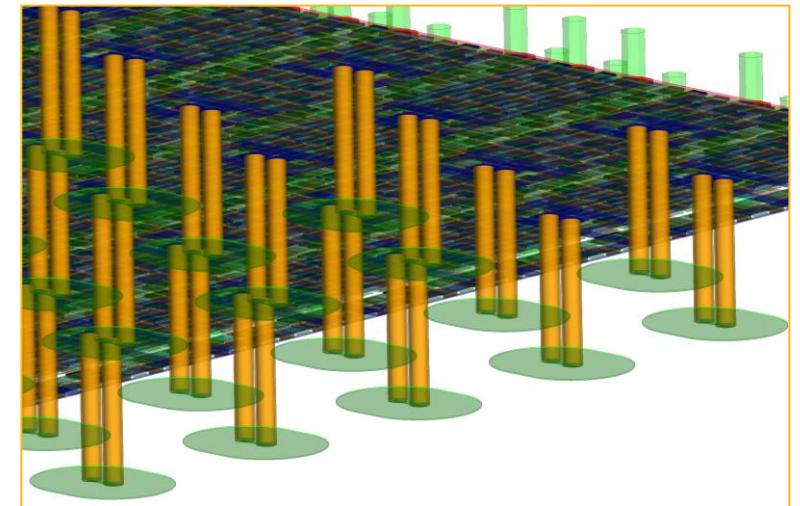
Attributes

Analysis

Etch
Rough
Roughness
Solver

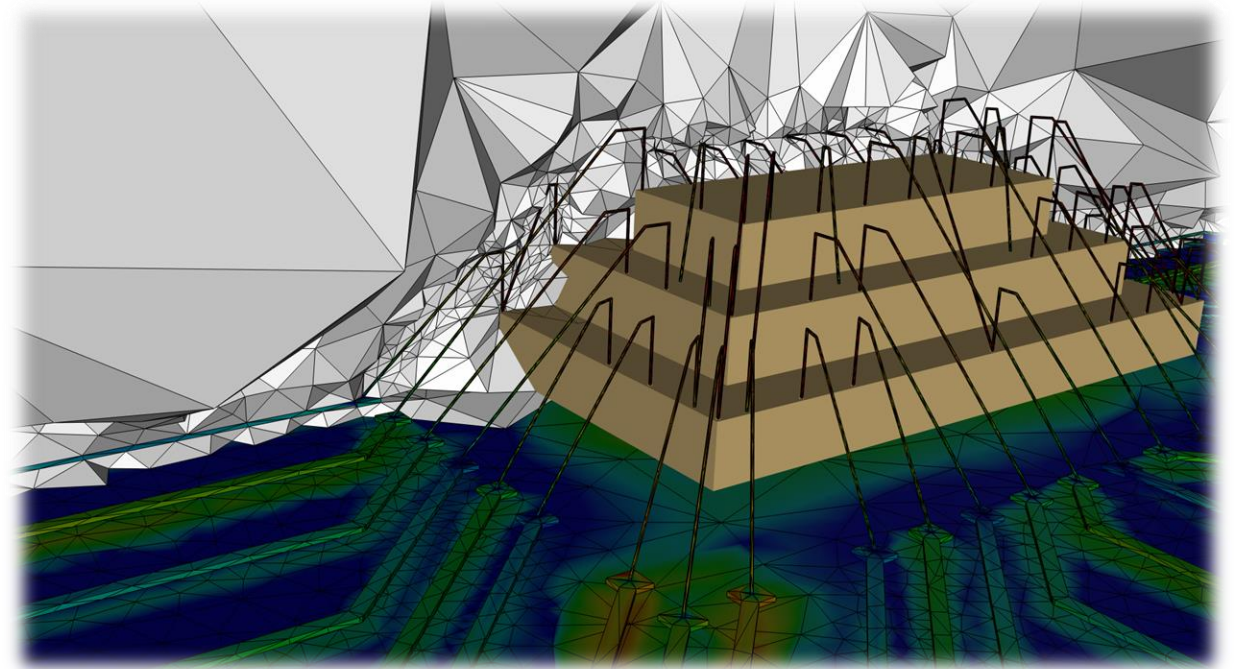
TSV

Thickness	Material
0.1um	silicon



Mesh Fusion Usability

- Phi+ available for Mesh Fusion [Beta]
 - Only for the top-level and Layout sub-designs
 - Improved meshing for assemblies with Phi-incompatible domains
 - Assemblies with bondwire packages
 - PCB's with connectors
 - Domains hosting complex envelopes



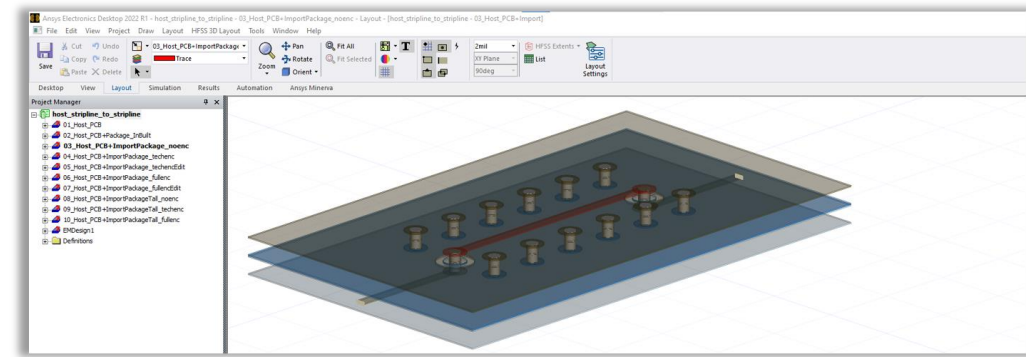
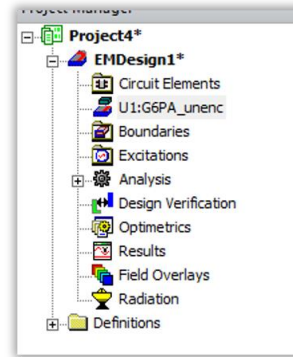
- Intersection check performance
- Robustness
 - Improved pre-processing

Time: 08/13/2021 10:24:52				
Initial Meshing				
Initial Mesh With Distributed Mesh Assembly				
Mesh Phi	00:09:51	00:09:51	8.18 G	1881059 tetrahedra [U1]
Mesh (MRL based)	00:02:46	00:02:45	8.23 G	1912366 tetrahedra [U1]
Phi Plus	00:15:28	00:26:21	7.38 G	4533487 tetrahedra [native] by 24 of cores
Mesh Coarsening	00:07:41	00:07:41	7.38 G	3345911 tetrahedra [native]
Mesh Assembler	00:30:39	00:30:39	7.25 G	0 tri + 5258277 tets
Refinement With Distributed Mesh Assembly				
Mesh Assembler	00:04:11	00:04:11	4.63 G	0 tri + 5208808 tets

3D Layout Component (Beta)

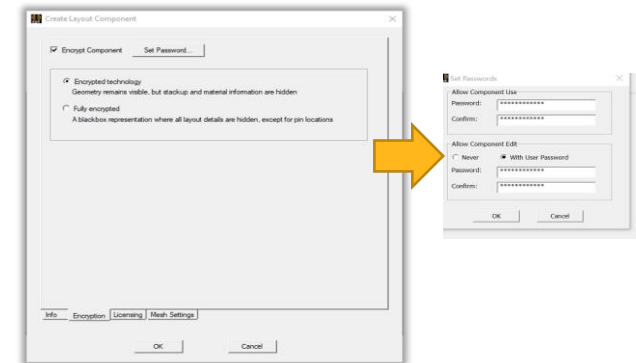
- Layout Component

- Any EDB can function as a component
- Encapsulated data handling



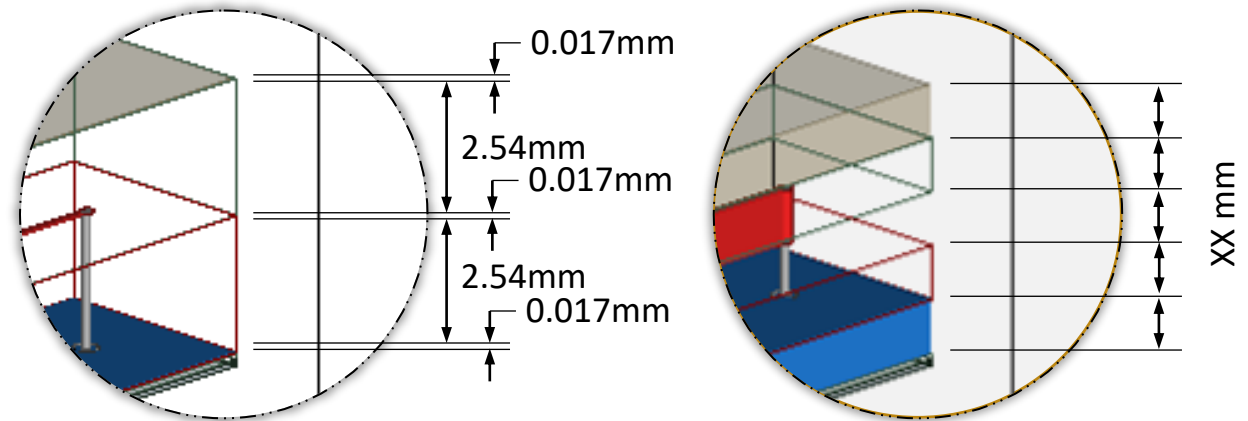
- Encrypted Technology

- Obfuscated stackup
- No material definitions available
- All data/mesh/solutions encrypted on disk



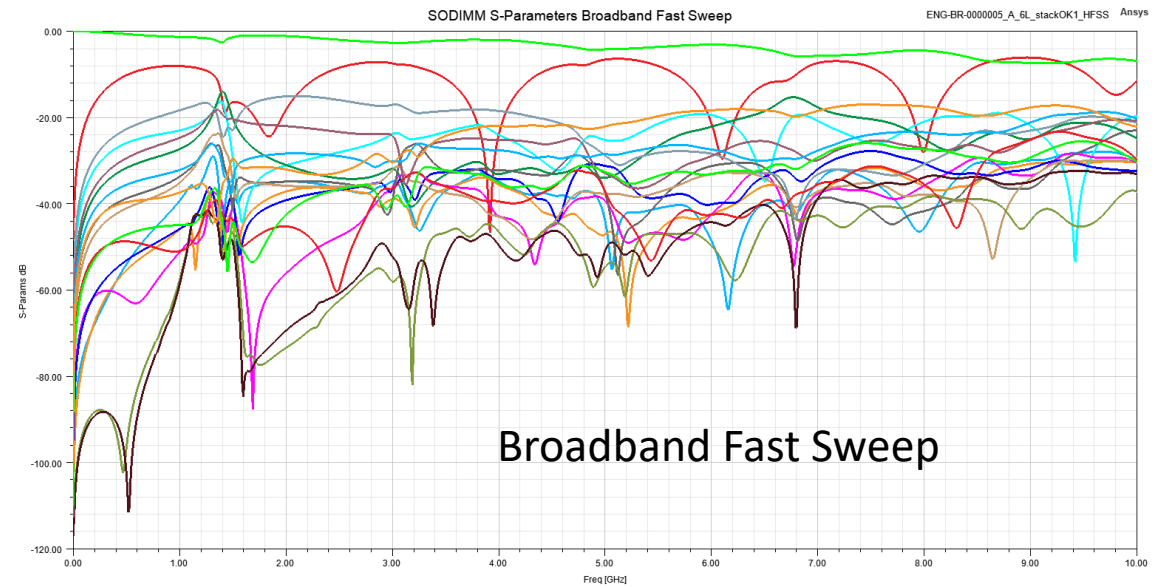
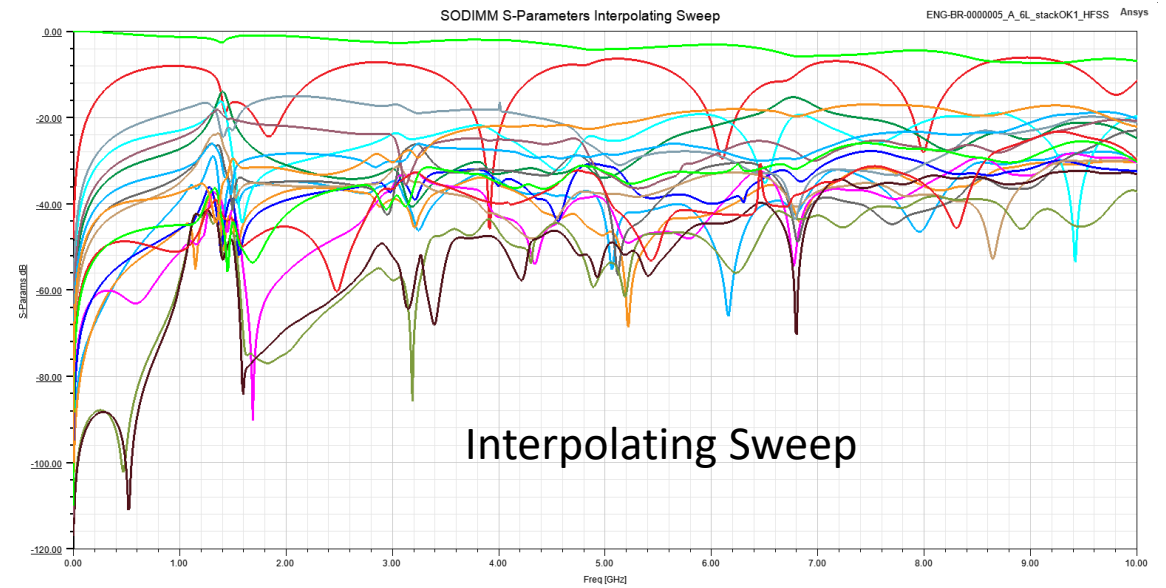
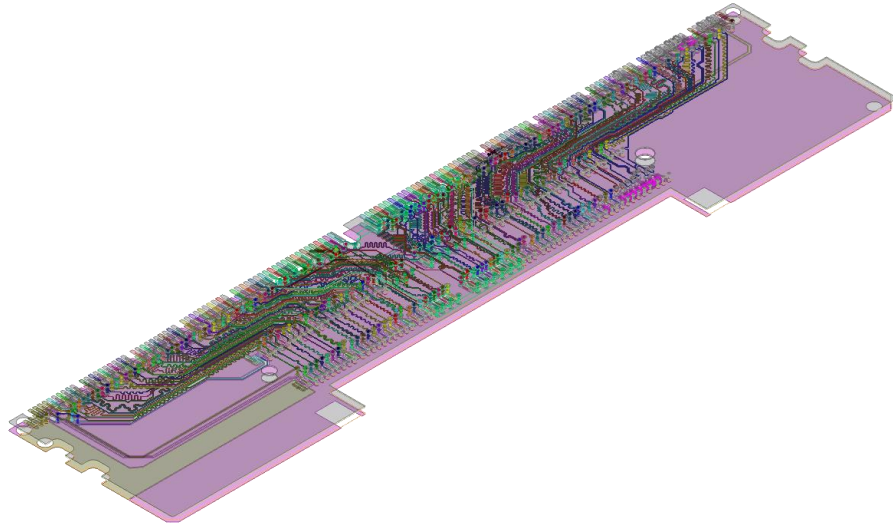
- Fully Encrypted

- Blackbox view
- Visibility of terminal locations only



Broadband Fast Sweep (Beta)

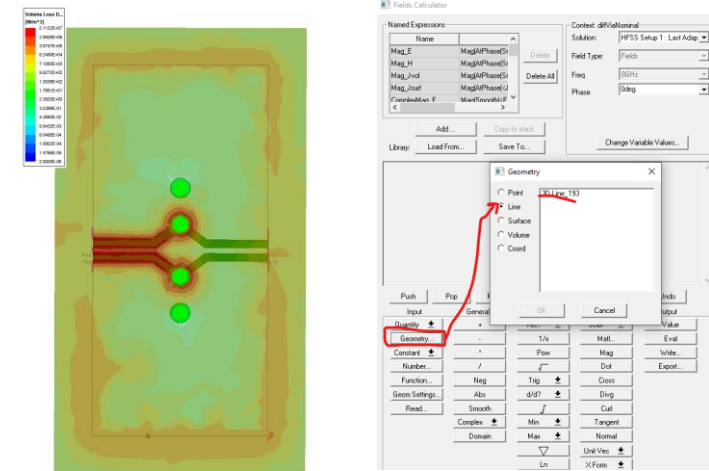
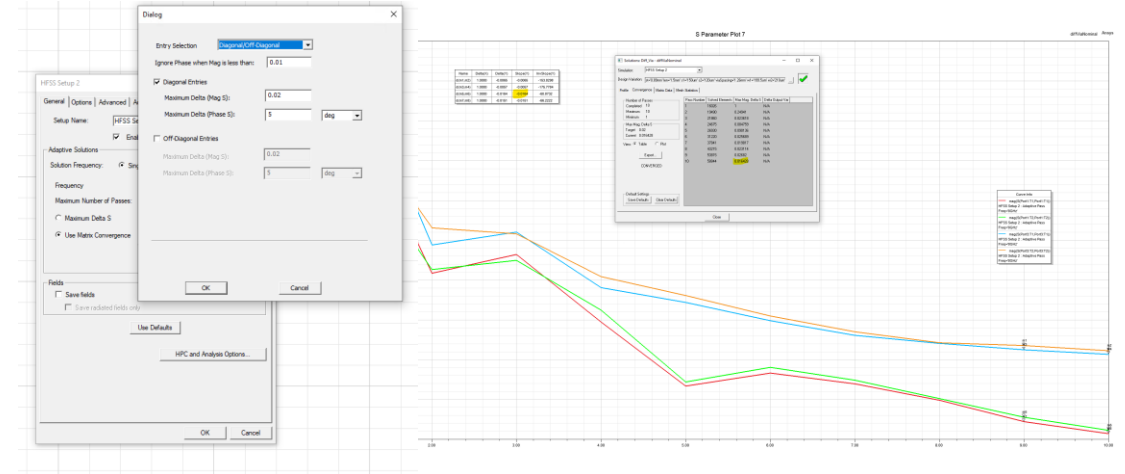
- Projection-based model order reduction
 - Uses derivatives of solution vectors as basis.
 - Uses automatic differentiation for derivatives of causal dielectrics, finite conductivity BC, etc.
- Excellent accuracy with fewer basis points



	Time	Basis points	Speed
Interpolating	3 hr, 50 min	113	1
Broadband Fast	2 hr, 8 min	24	1.79

Layout Usability Enhancements – 2022R1

- New convergence criteria support
 - Matrix
 - Output variables as functions of Differential Pairs
- 3D Component Display in Project Tree
 - Selection, Edit Definition, Edit Properties, Visibility
- Fields Post-Processing
 - Volume loss density
 - 3D-Line types available for Fields Calculator
 - Performance improvements

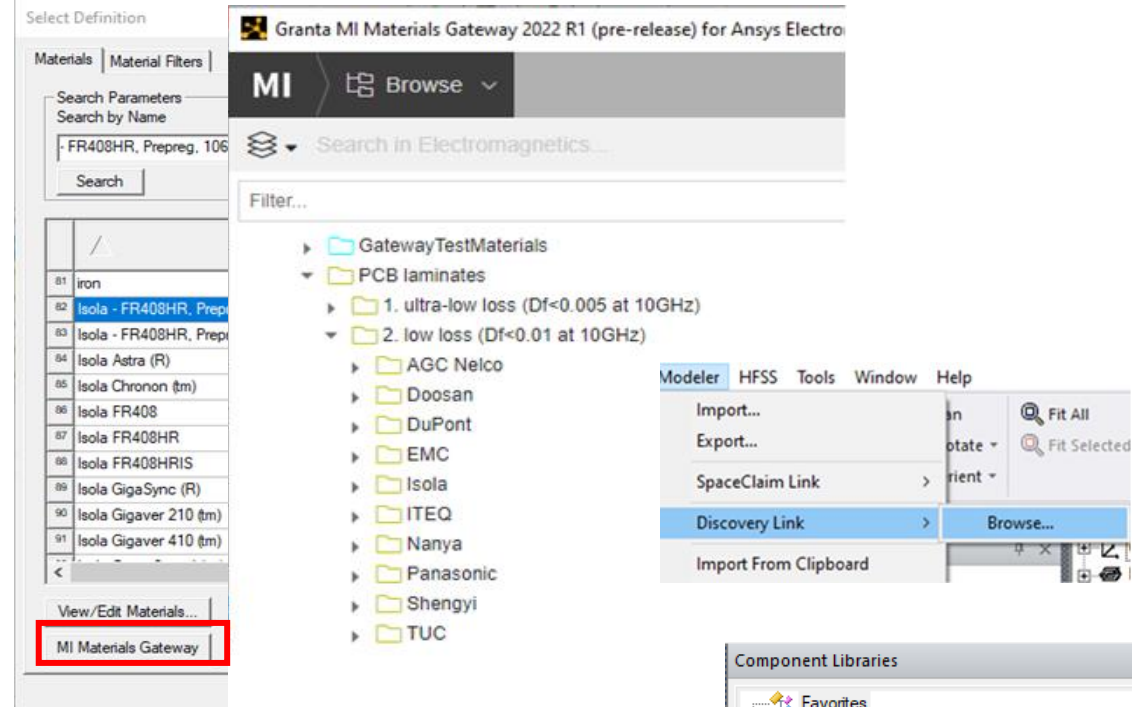


Ansys Electronics Desktop

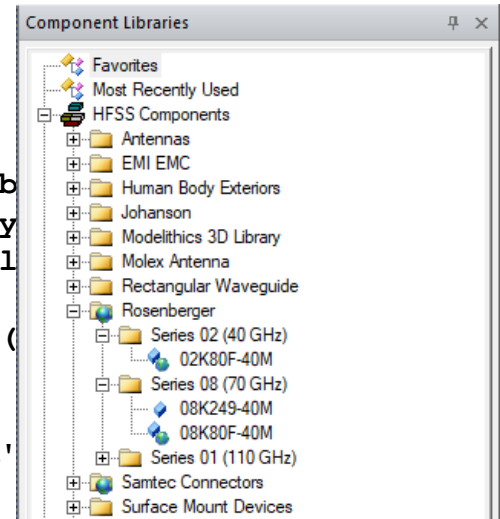
Ansys

ANSYS Electronics Desktop

- Granta MI Materials Gateway
 - Granta Material Gateway integrated in AEDT material browser
- 3D Component Agents
 - Identical tree hierarchy as installed components
- Object oriented property scripting
 - New modules: Mesh operations, 3D component array, Field overlays
 - Functions to access SI and evaluated values
- 3D Modeler - Discovery link (Beta)

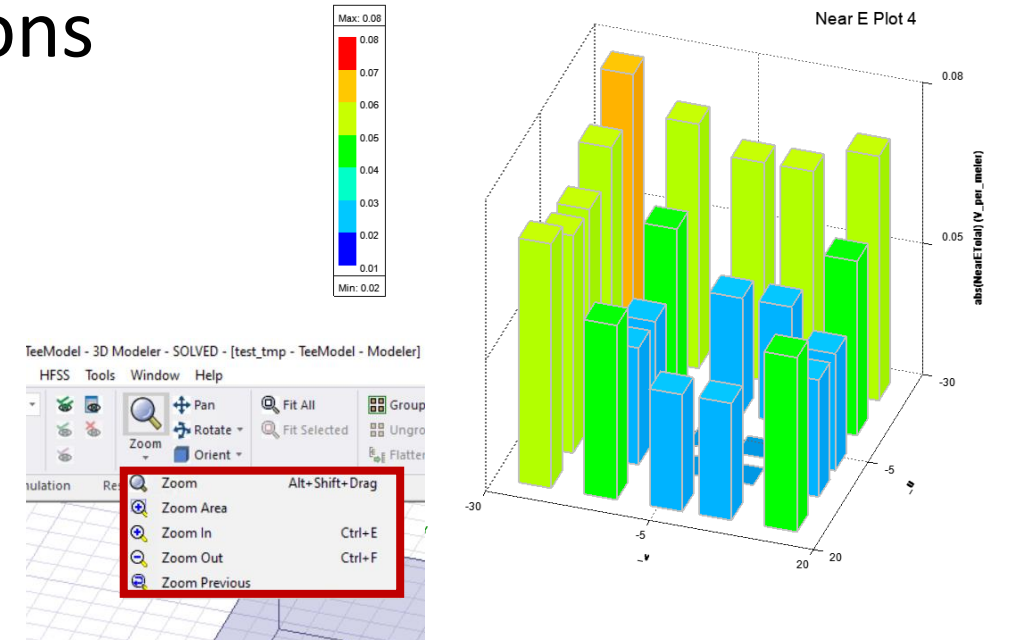


```
>>> oDesign.GetChildNames ()
['Boundaries', 'Excitations', 'Hyb
Elements', 'Model', 'Mesh', 'Analy
'Port Field Display', 'Field Overl
'Results', '3D Modeler']
>>> oModel=oDesign.GetChildObject (
>>> oModel.GetChildNames ()
['A']
>>> oA = oModel.GetChildObject('A'
>>> oA.GetPropNames ()
['Name', 'Type', 'Visible', 'Render', 'Render/Choices',
'A Vector', 'A Vector/Choices', 'B Vector', 'B
Vector/Choices', 'A Cell Count', 'B Cell Count',
```

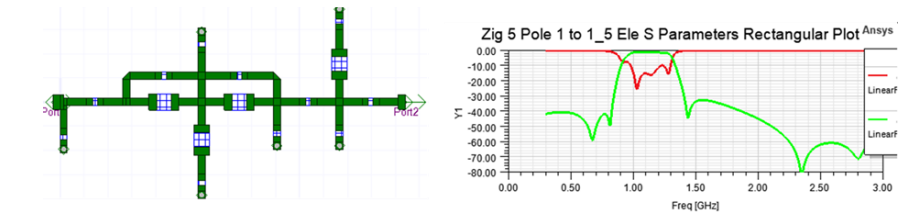


Graphics, Post processing, FilterSolutions

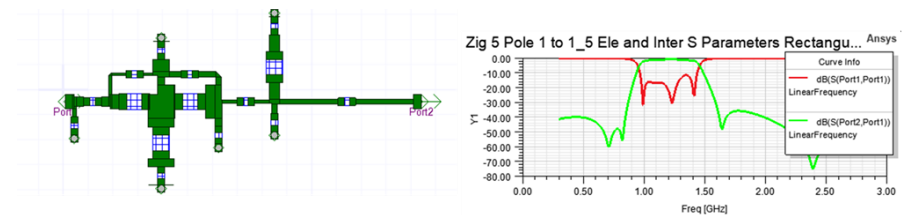
- 3D Rectangular Bar plot type
- Enhanced zoom controls in 3D modeler and plots
- Improved handling of post-processing variables in Optimetrics
- Automated Discrete Optimization [Beta]
 - Rapid and Accurate Lumped Element Filter Design
 - Utilizes Ansys FilterSolutions, Circuits, and AEDT Optimizers
 - Support for Modelithics Library



First Pass Optimizes Only the Elements



Second Pass Optimizes Interconnects



The Ansys logo is positioned on the left side of the slide. It features a yellow slanted bar to the left of the word "Ansys" in a bold, black, sans-serif font.

Ansys

