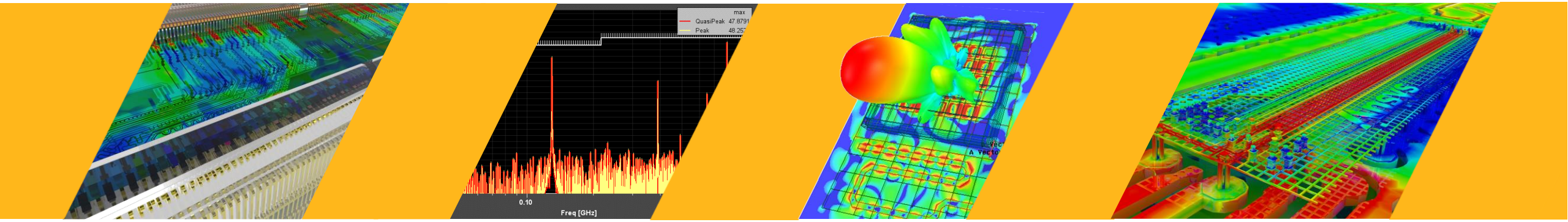
Release 2023 R1 Highlights

Ansys High Frequency Electromagnetics

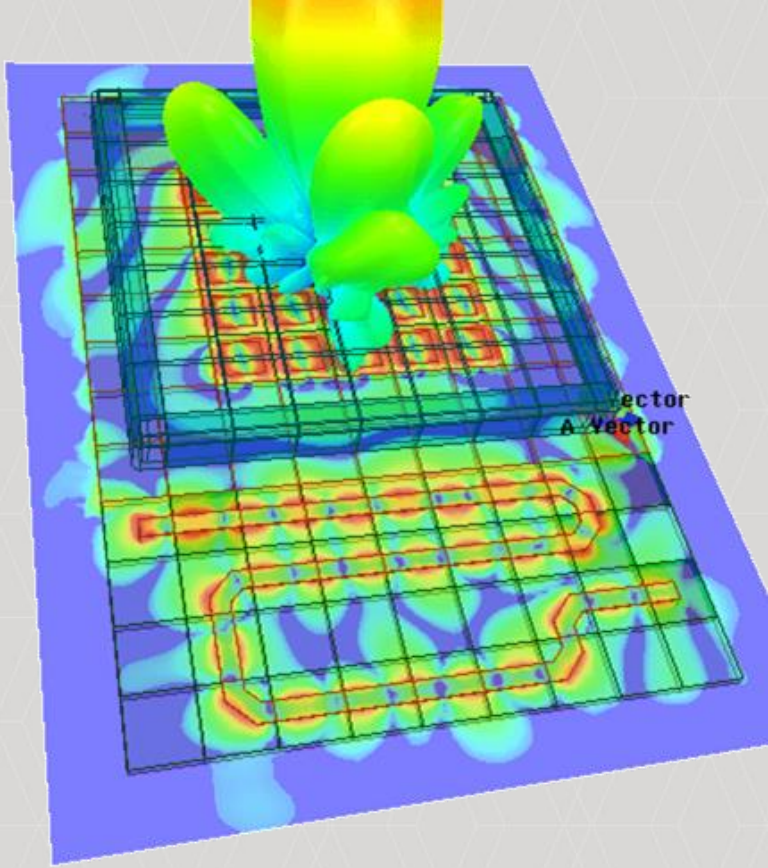
Ansys HFSS, SBR+, EMIT, HF Circuit

Ansys High Frequency Electromagnetics 2023 R1 Highlights



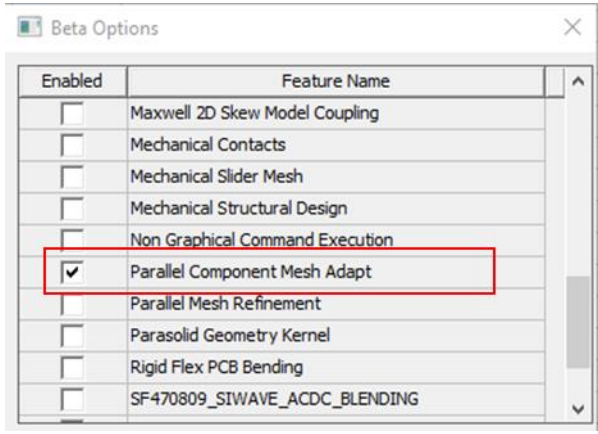
- ✓ **Parallel component adaptive** for 3D component arrays (Beta)
- ✓ Improved **workflows for layout component**
- ✓ **Arbitrary backdrill** depth in HFSS 3D Layout
- ✓ Improved **HPC performance** for **distributed mesh fusion** and **domain solver for large arrays**
- ✓ New **EMI receiver component** and new adaptive time stepping algorithm for nonlinear circuits
- ✓ **Custom arrays**, **file based near field** and **PTD/UTD support for advanced doppler** in SBR+

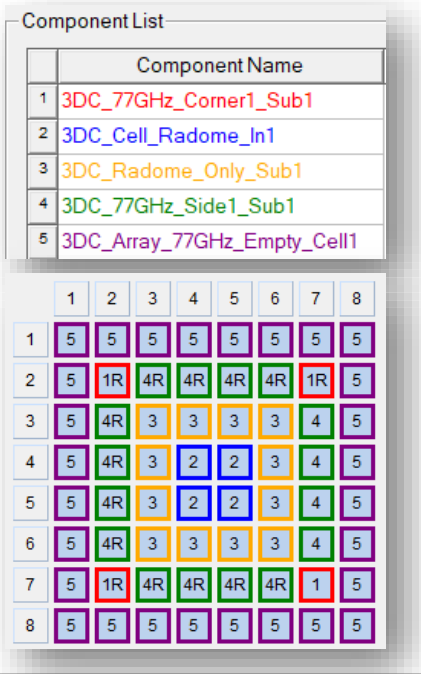
HFSS 3D

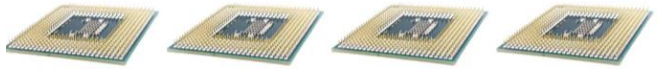


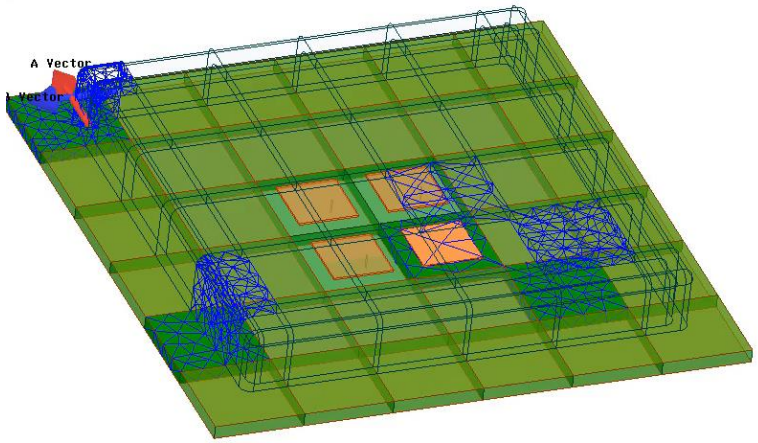
Parallel Component Adapt for 3D Component Array

- Traditionally, HFSS uses all available cores to adapt the mesh of each 3D component of an array in series
- In 2023 R1, HFSS can perform the adaptive mesh refinement of the 3D components of an array in parallel







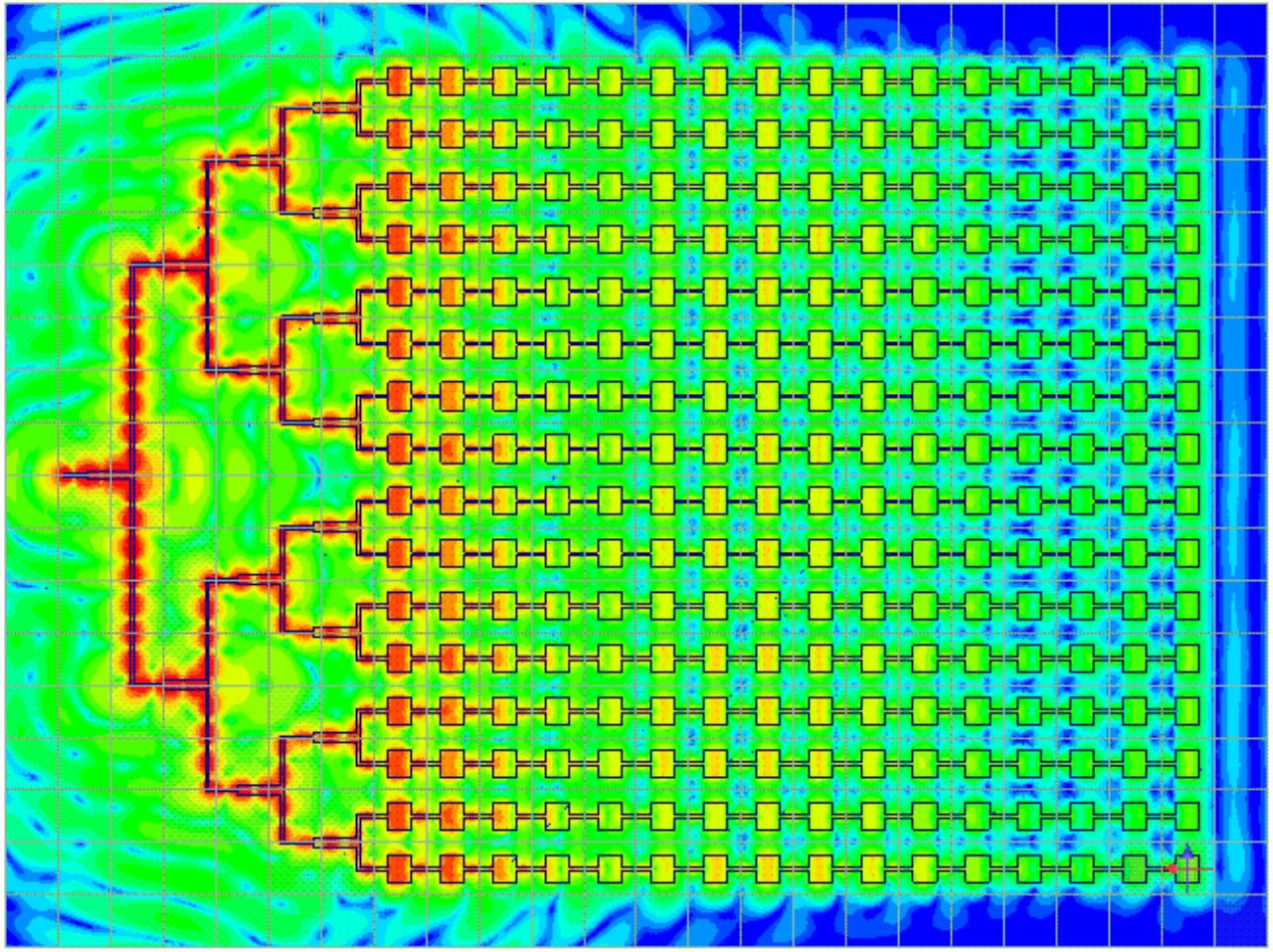


ADAPTIVE PASS 1

Parallel component adaptive for 3D component array [Beta]

- 16 x16 array with feed network
  - Array with 432 Elements
  - 26 Individual Components
  - Adaptive mesh 42% faster

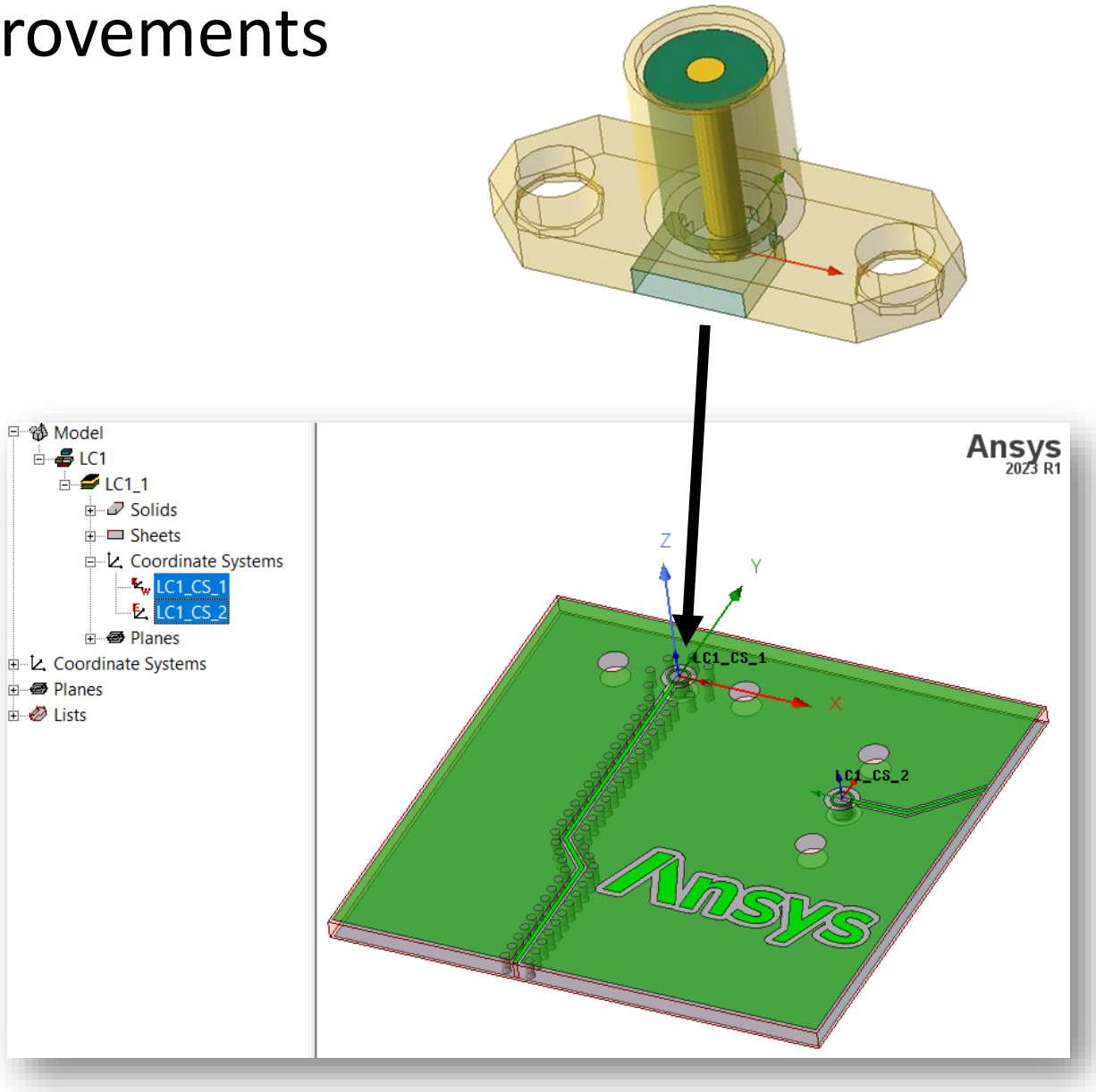
Delta S	# of passes	12 Core Adaptive Mesh	
		Sequential	Parallel
0.02	5	3:31	2:29



Layout Component Workflow Improvements

- Easier Component Placement
  - Layout Reference Coordinate System Available
- Mesh Fusion enabled
- Layout Component's bounding box and ports invoked as geometry
  - Enables moving and snapping entire component
- Layout Component is editable from inside target HFSS design
- Visualization settings

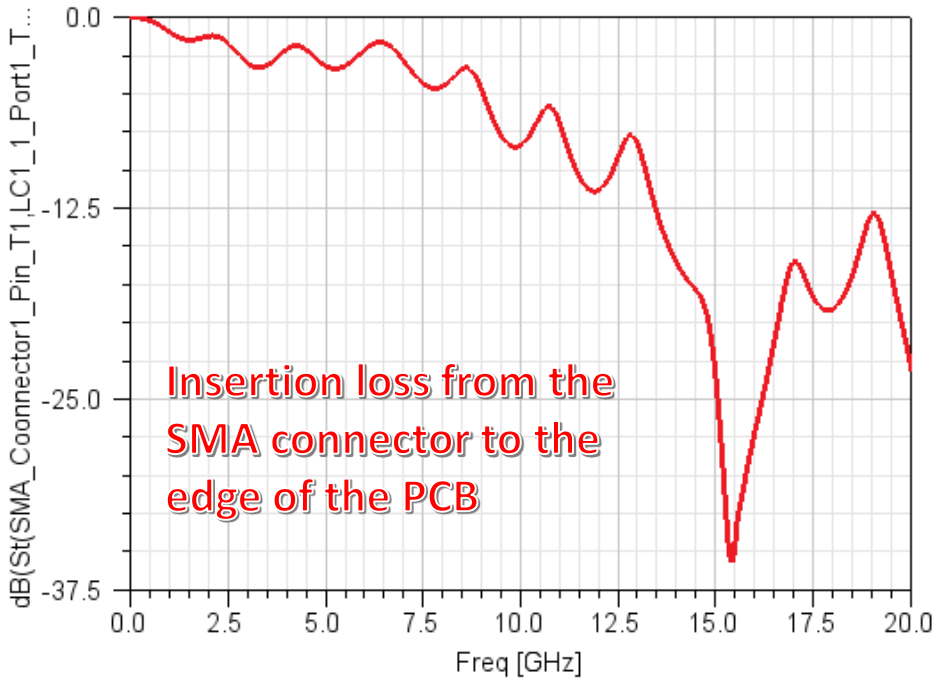
  Stack up layers or individual nets

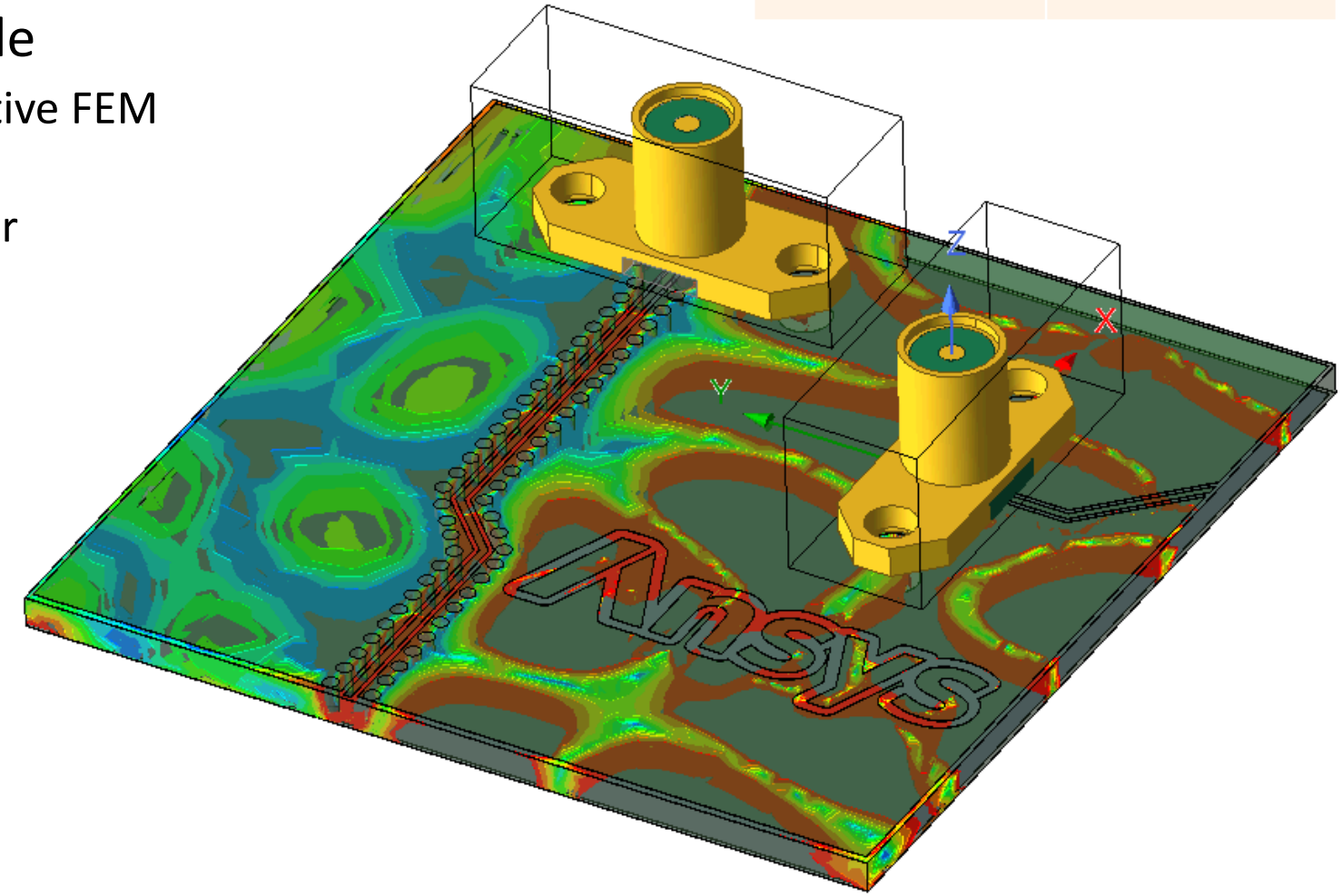


Layout Component Workflow Improvements

32 cores	
Time	Max RAM
00:14:04	2.09 GB

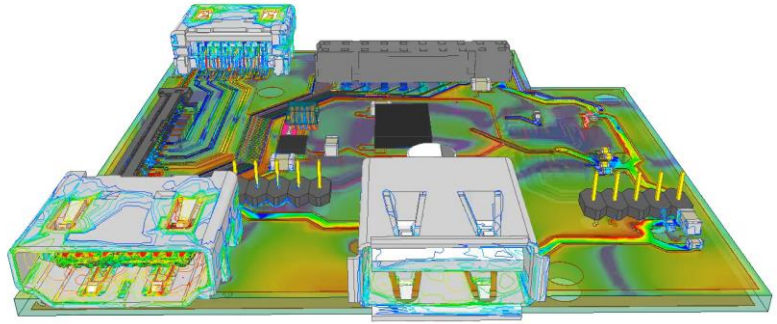
- SMA connector on board example
  - Mesh fusion with 3 domains plus native FEM
    - Layout component and 2 SMA connectors
  - Mesh fusion with new iterative solver





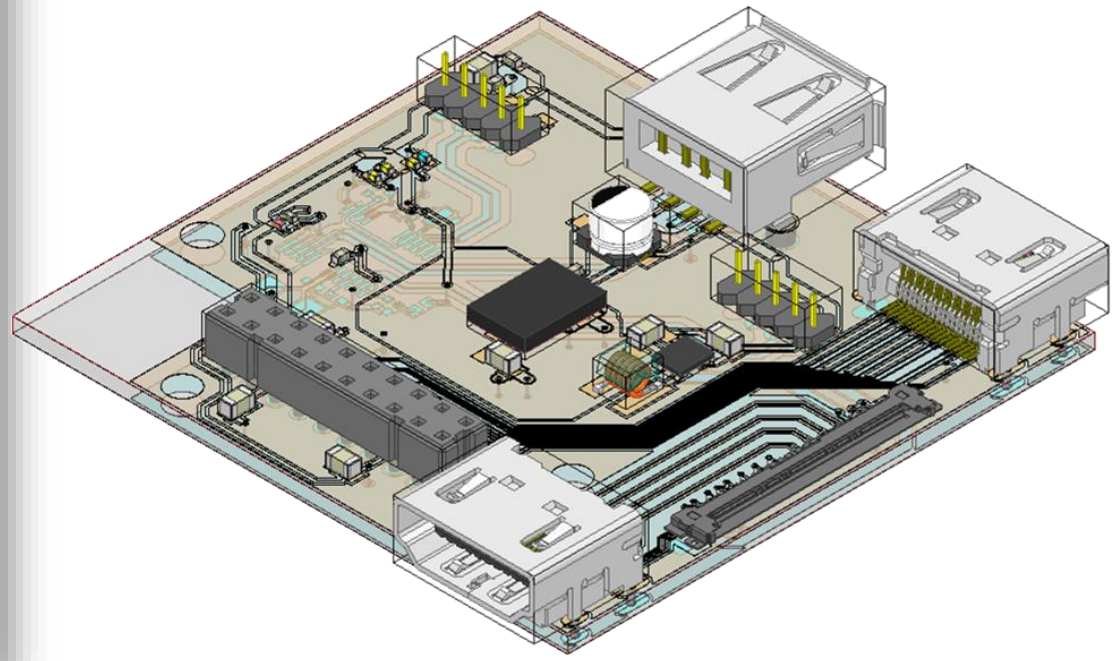
Layout Component Workflow Improvements, cont.

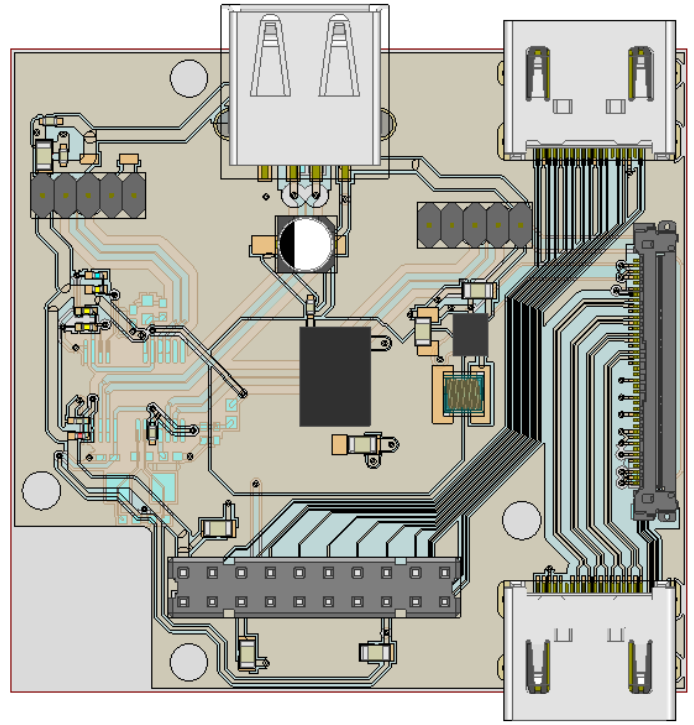
- Full PCB assembly
  - Mesh fusion with 29 domains plus native FEM



Mesh Fusion(Beta) Settings

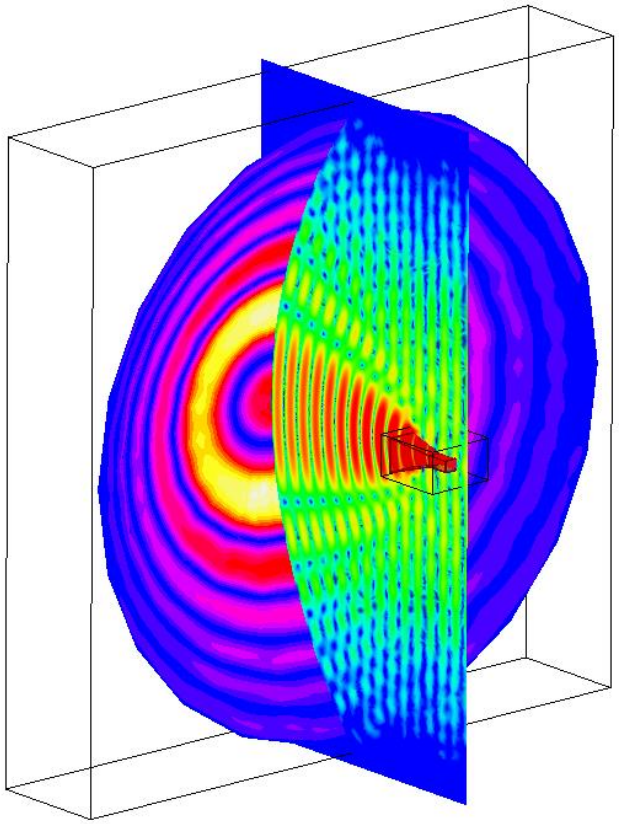
Component Name	Meshing Type	Enable
10x2_Connector1	Volume - Classic	☑
Bulk_Capacitor1	Volume - Classic	☑
Capacitor_1_1	Volume - Classic	☑
Capacitor_1_2	Volume - Classic	☑
Capacitor_1_3	Volume - Classic	☑
Capacitor_1_4	Volume - Classic	☑
Capacitor_1_5	Volume - Classic	☑
Capacitor_1_6	Volume - Classic	☑
Capacitor_1_7	Volume - Classic	☑
Capacitor_2_1	Volume - Classic	☑
Capacitor_2_2	Volume - Classic	☑
Capacitor_2_3	Volume - Classic	☑
Capacitor_2_4	Volume - Classic	☑
Capacitor_3_1	Volume - Classic	☑
HDMI_Connector1	Volume - Classic	☑
HDMI_Connector2	Volume - Classic	☑
Header5_Male1	Volume - Classic	☑
Header5_Male2	Volume - Classic	☑
Inductor1	Volume - Classic	☑
LC3_1	Volume - Phi	☑
Resistor_1_1	Volume - Classic	☑
Resistor_2_1	Volume - Classic	☑
Resistor_2_2	Volume - Classic	☑
Resistor_2_3	Volume - Classic	☑
Resistor_3_1	Volume - Classic	☑
Ribbon_Cable_Connector1	Volume - Classic	☑
U100_1	Volume - Classic	☑
U101_1	Volume - Classic	☑
USB_Connector1	Volume - Classic	☑





Iterative Solver for Mesh Fusion

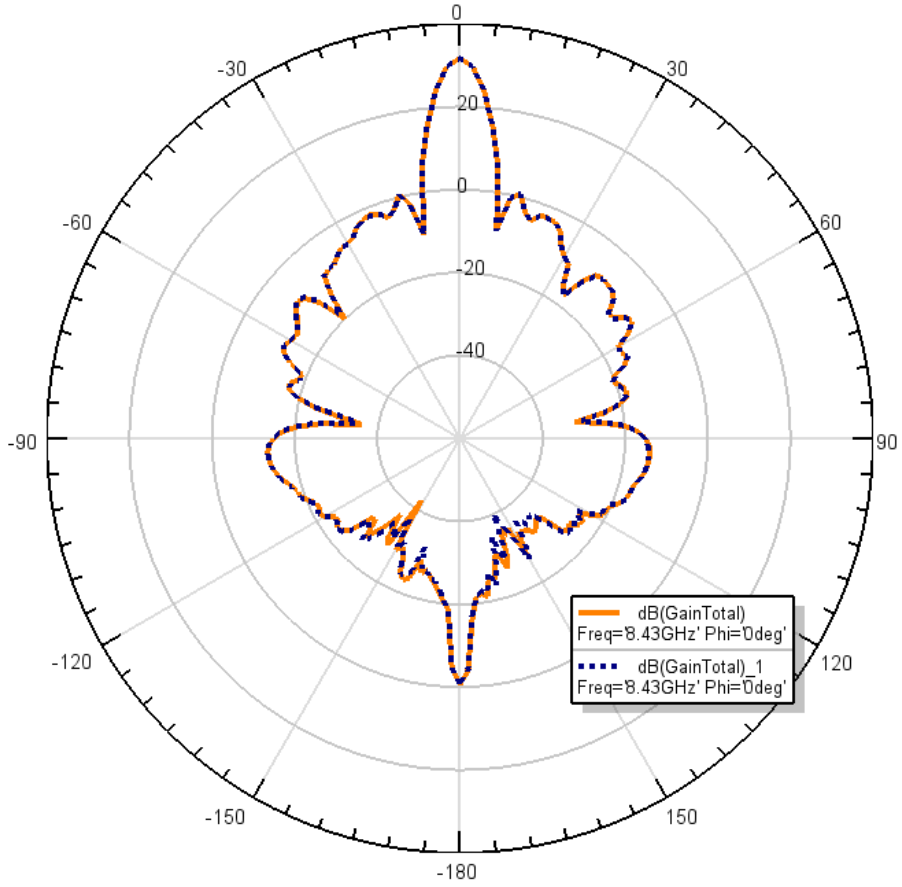
- Iterative solver now available for Mesh Fusion



Horn antenna with reflector

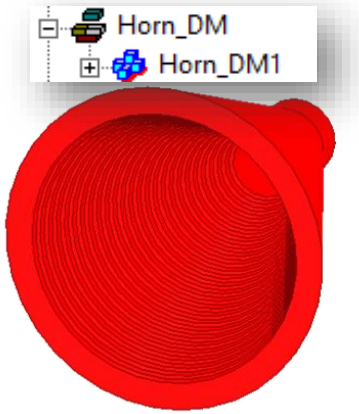
32 cores - Mesh fusion 2 domains			
direct		iterative	
00:49:31	113 GB	00:29:07	52.1 GB

Iterative is 42% faster using 54% less RAM

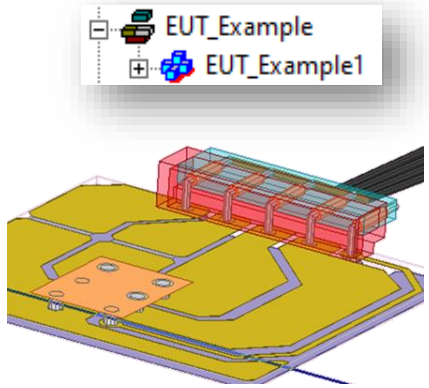


Modal Port in Terminal Design

- Allow both modal and terminal wave/lumped port in terminal solution type
- Allow both modal and terminal 3D components in a terminal solution type
- If there are modal ports in the design, edit source excitation switches to power

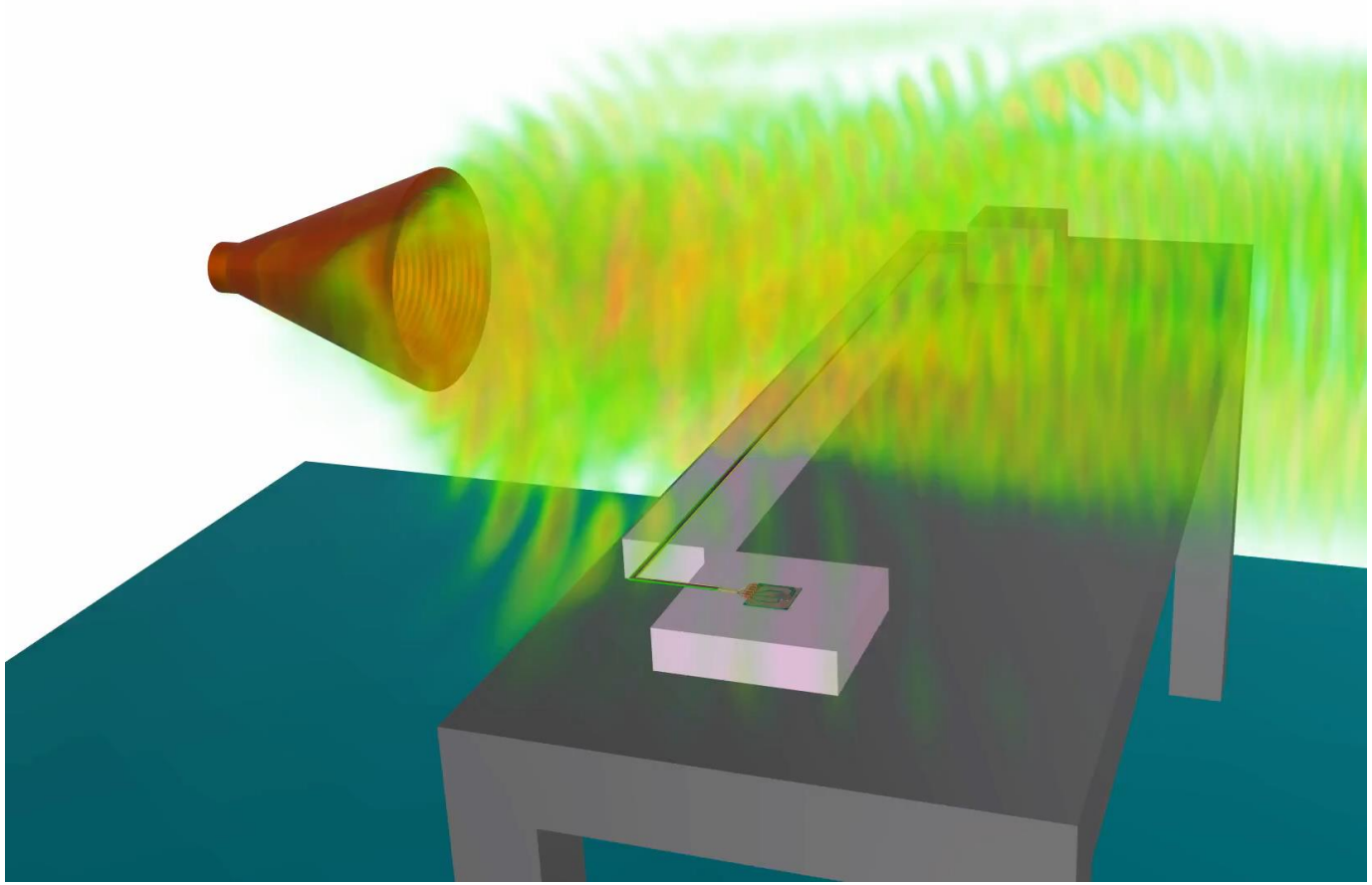


DM



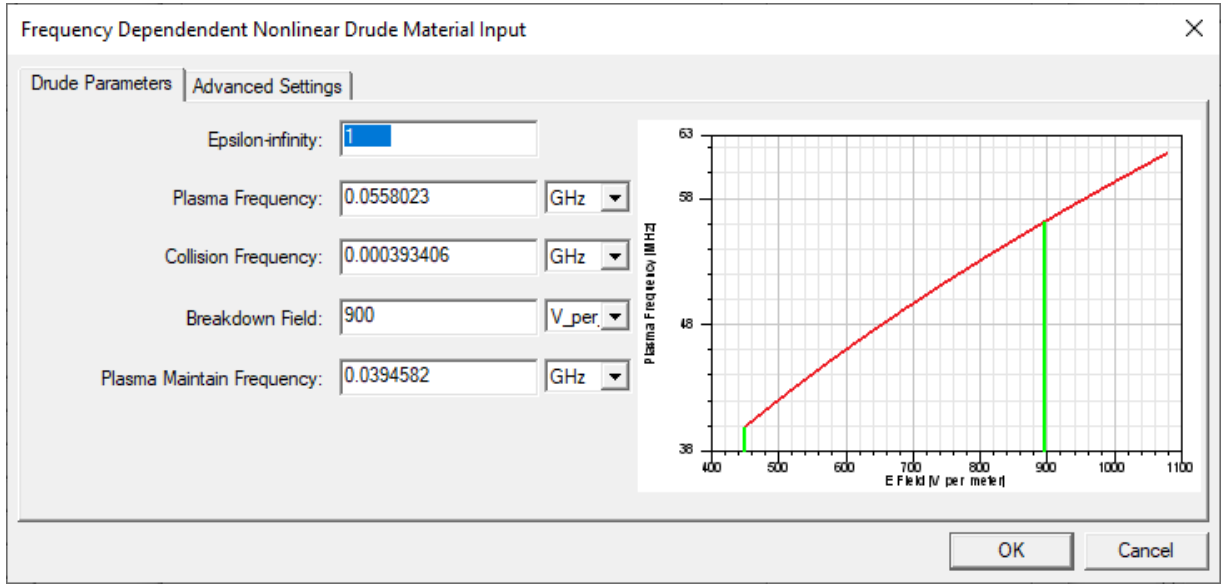
DT

Radiated Immunity setup with Driven Modal and Driven Terminal components

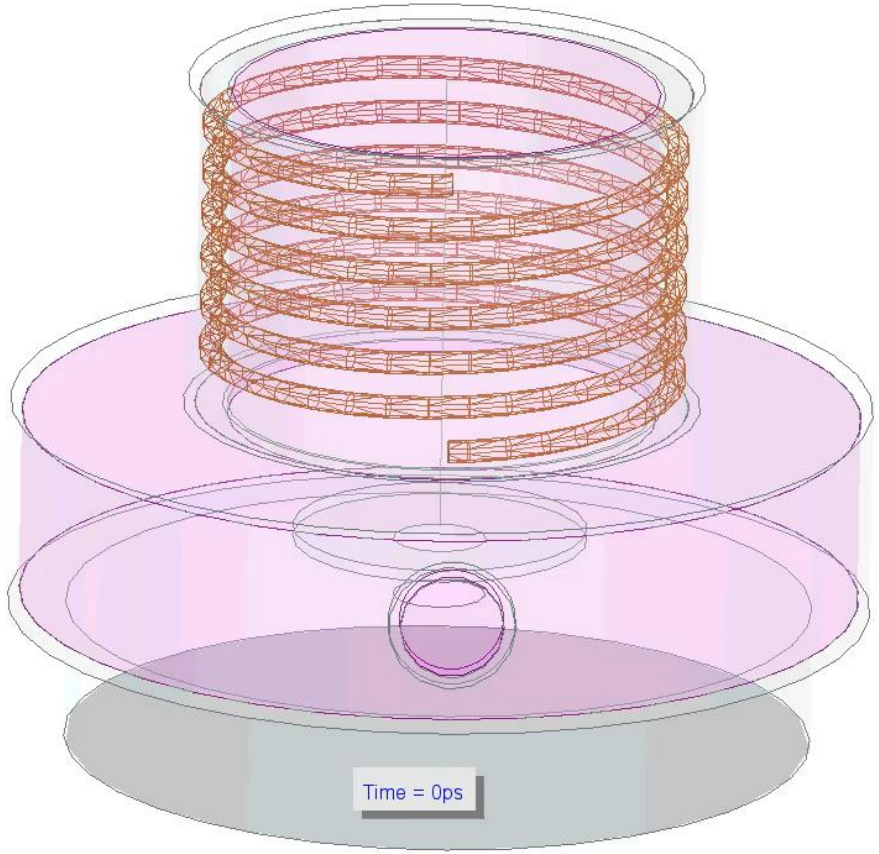


Nonlinear Drude and Plasma Density Calculation for HFSS Transient

- Solution for plasma enhanced chemical vapor deposition (PECVD) and microwave-induced plasmas
  - Where dielectric dispersion is time-dependent
- Simulate electromagnetic wave propagation in a non-magnetized plasma
  - Predict the spatial distribution of plasma density



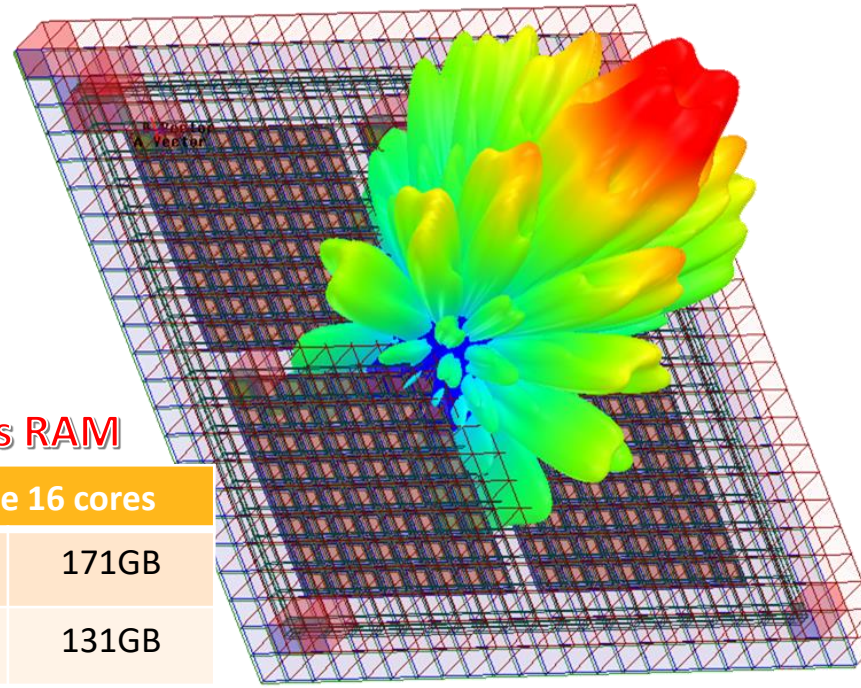
Plasma Density on a
13.56MHz ICP CVD Chamber with Oxygen



HFSS HPC/Performance

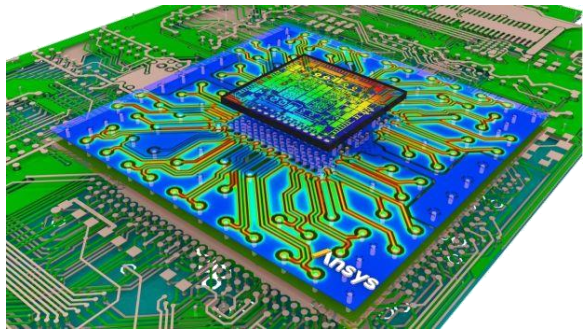
- Accelerated Mesh Fusion Solver
  - Multi-node distributed matrix assembly and field recovery including 3D component array
  - Improve distributed matrix solve performance
- Improve iterative domain solver speed for very large arrays
  - Improve speed by reducing the number of iterations
- AMD Math Library for Direct Matrix Solver
  - Full release
  - Automatic detection of CPU vendor, math library, used when AMD CPU is detected

2.4x speedup w/o saving fields



25% faster w/ 24% less RAM

Ver	# iter	1 machine 16 cores	
22.2	29.9	03:08:59	171GB
23.1	21.3	02:22:03	131GB



Complex Package, representative image

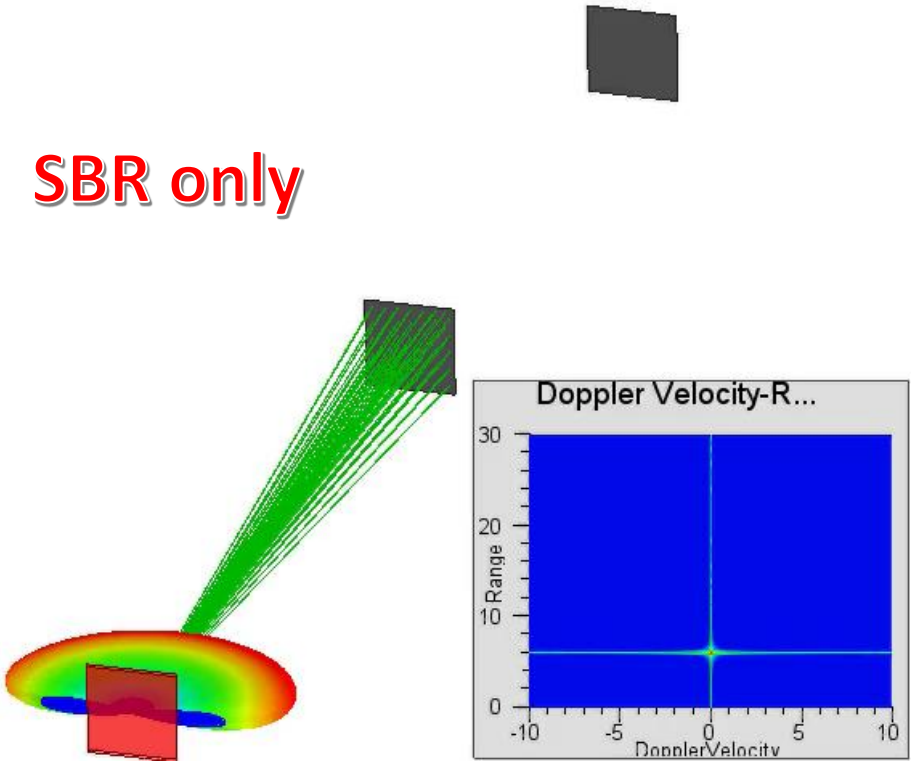
Num Cores	Without AMD lib	With AMD lib
8	0:17:46	0:09:45 (1.82x)
16	0:11:04	0:06:59 (1.58x)
32	0:08:13	0:05:42 (1.44x)

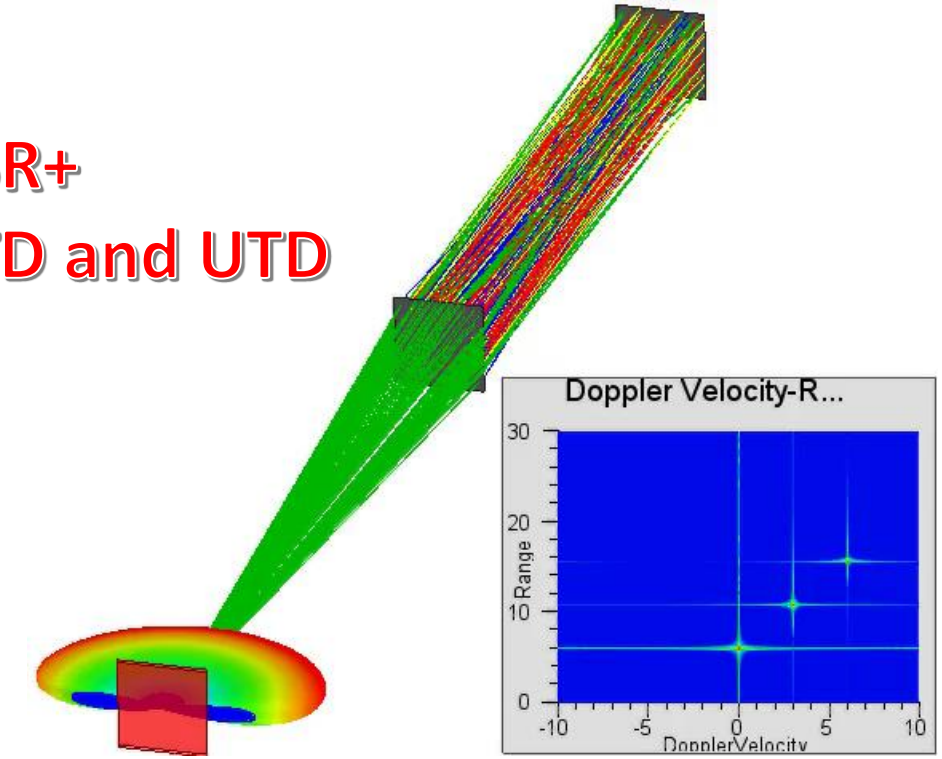
- 44% to 82% faster

HFSS SBR+

PTD and UTD for ADP

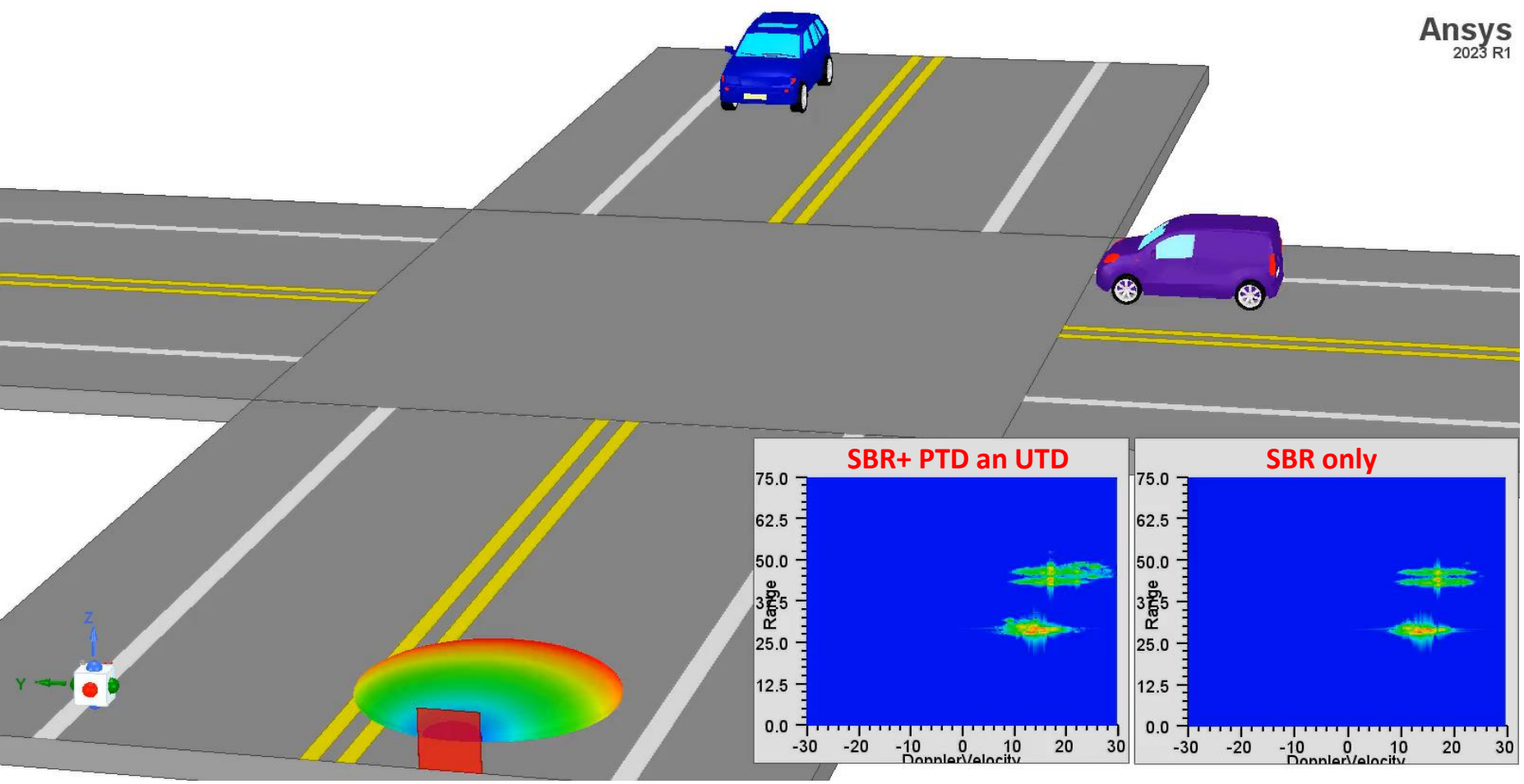
- PTD and UTD are available in generalized SBR+
  - 2023 R1 HFSS adds PTD and UTD support for ADP mode
- Two 1mx1m metal plates example:

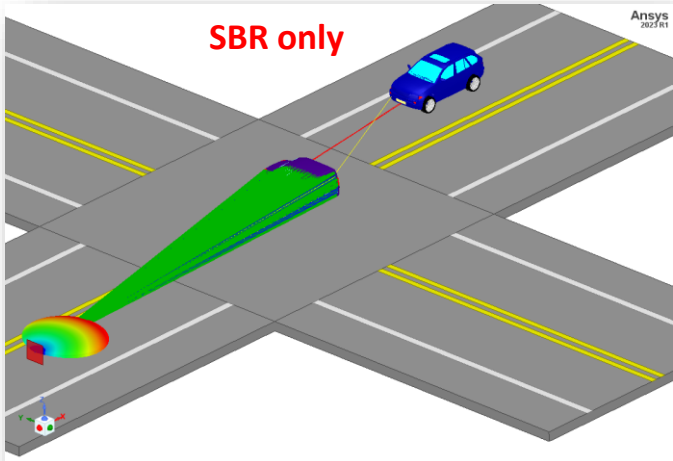


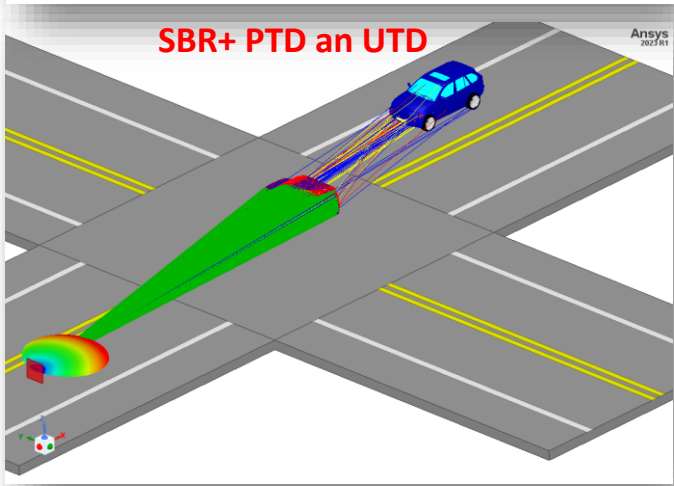


PTD and UTD for Accelerated Doppler Processing (ADP)

- Intersection demo:

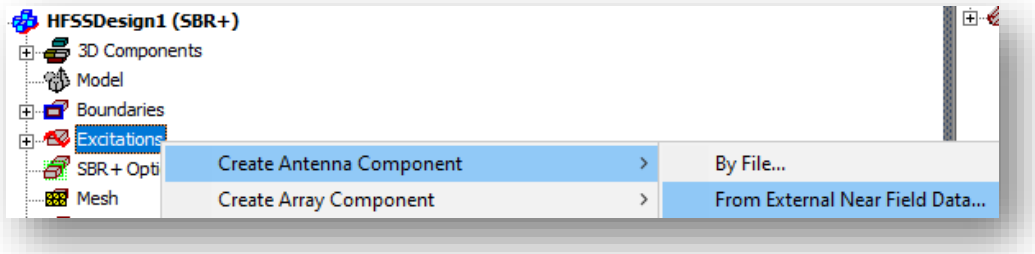


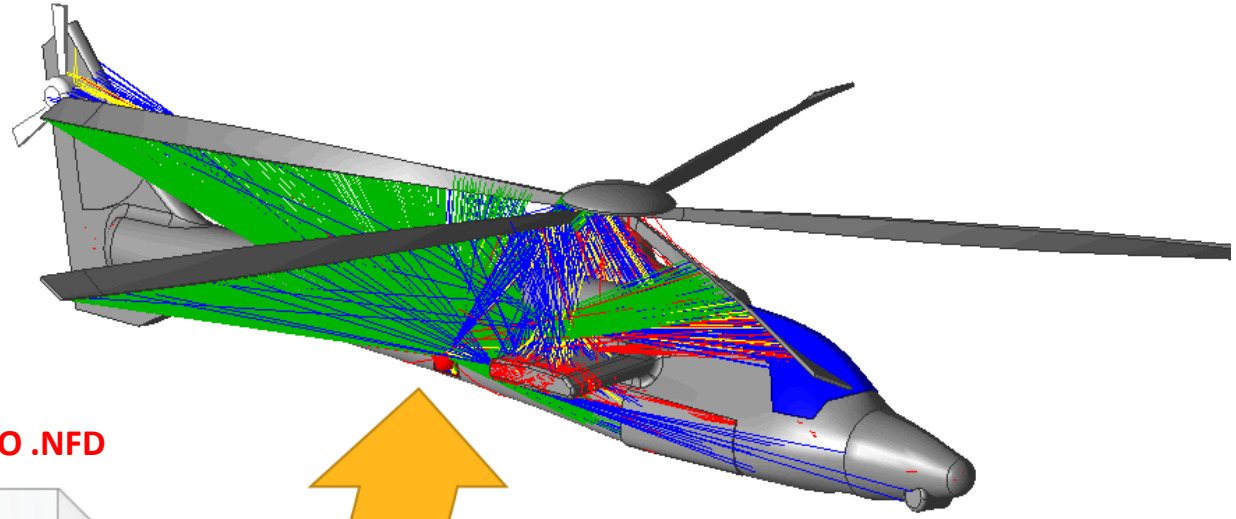




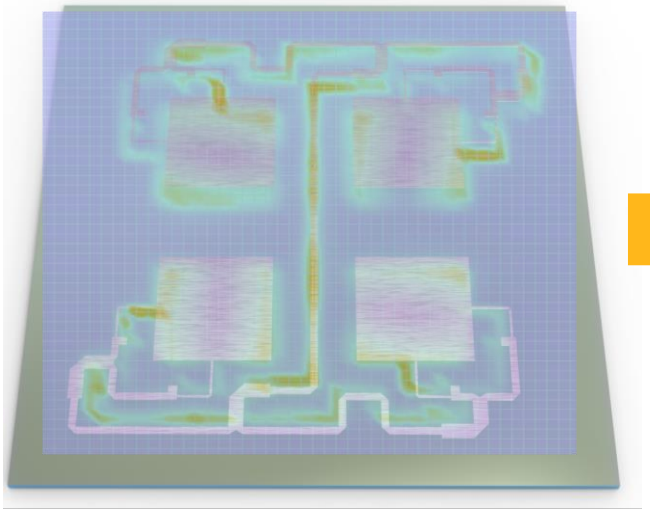
File-based near field antenna for SBR+

- Similar streamlined procedure as HFSS design
- Integrated with SBR+ functionalities

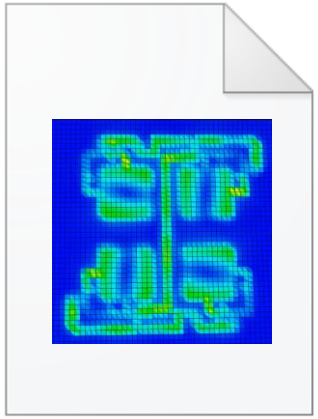




NEAR FIELD DATA



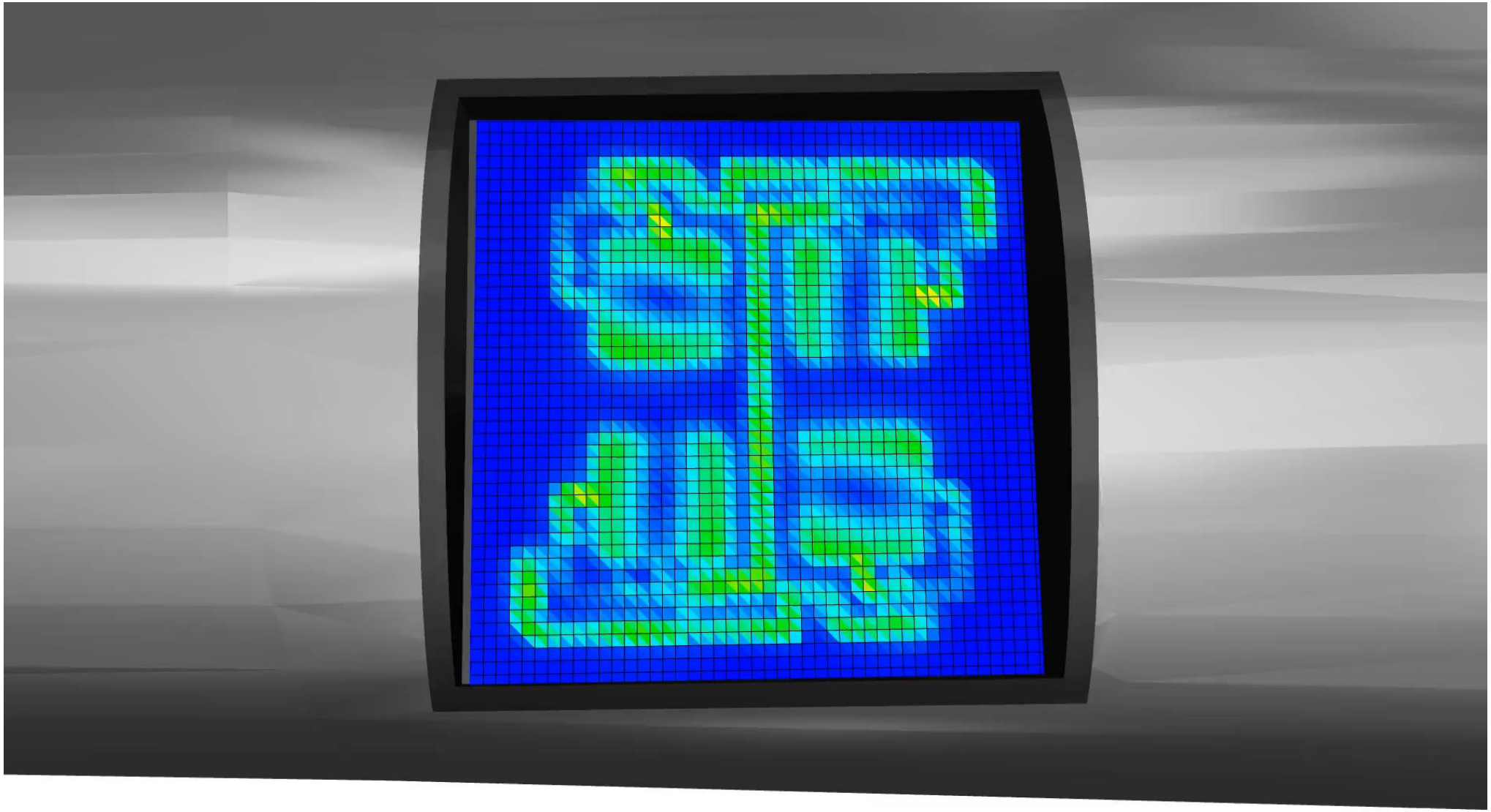
CONVERT TO .NFD



Patch_Array.nfd

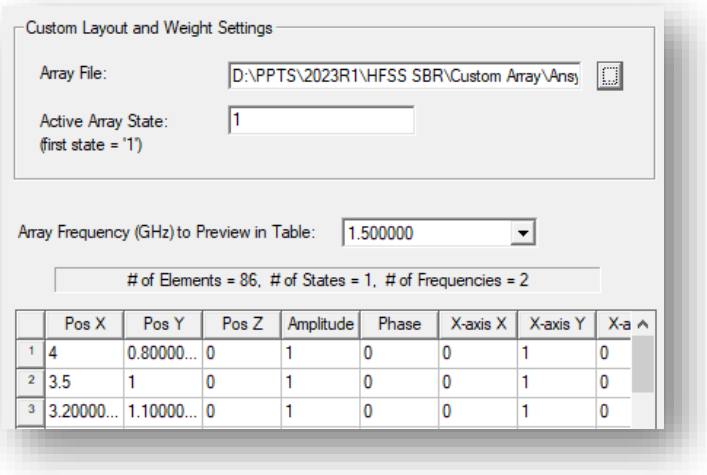
PLACE NFD ON
SBR+ PLATFORM

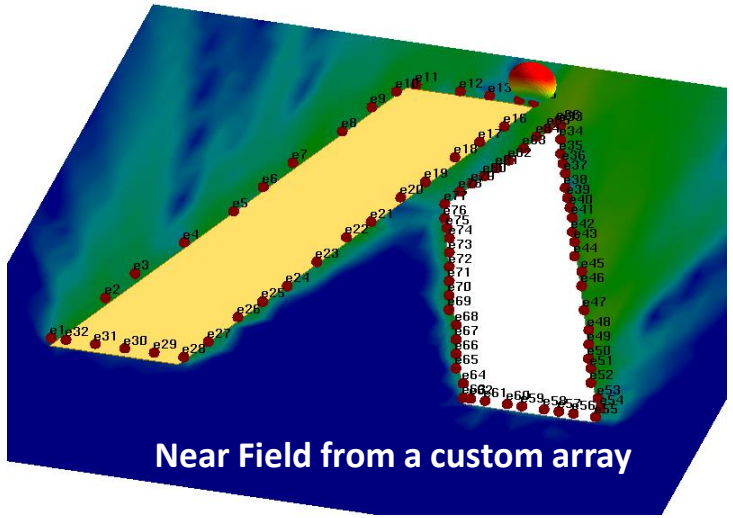
File-based Near Field Antenna for SBR+ Design



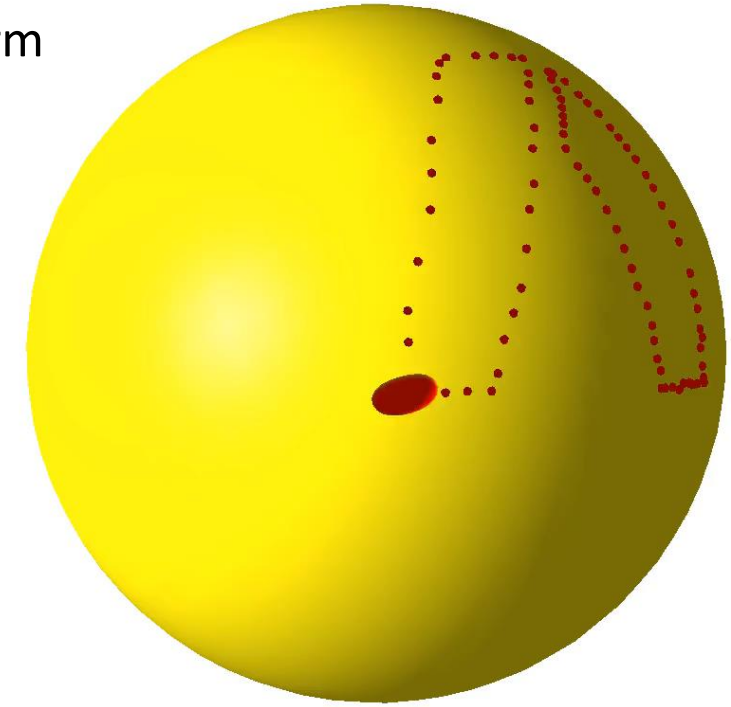
HFSS SBR+ Custom Array

- Add support for creation of custom (file-based) parametric arrays in HFSS SBR+ solution type
  - Uses Savant legacy *.sarr file format
  - Specifies array per-element locations and per-element complex weights
  - Can be placed conformal to the geometry and support element transform operations (X/Y/Z offsets, and phi/theta/psi rotations)



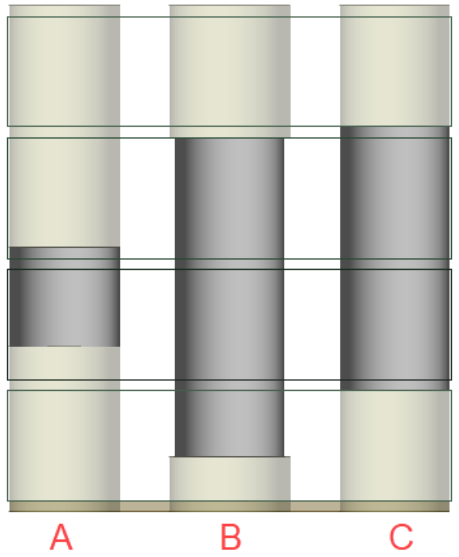


Array elements conformal to a sphere



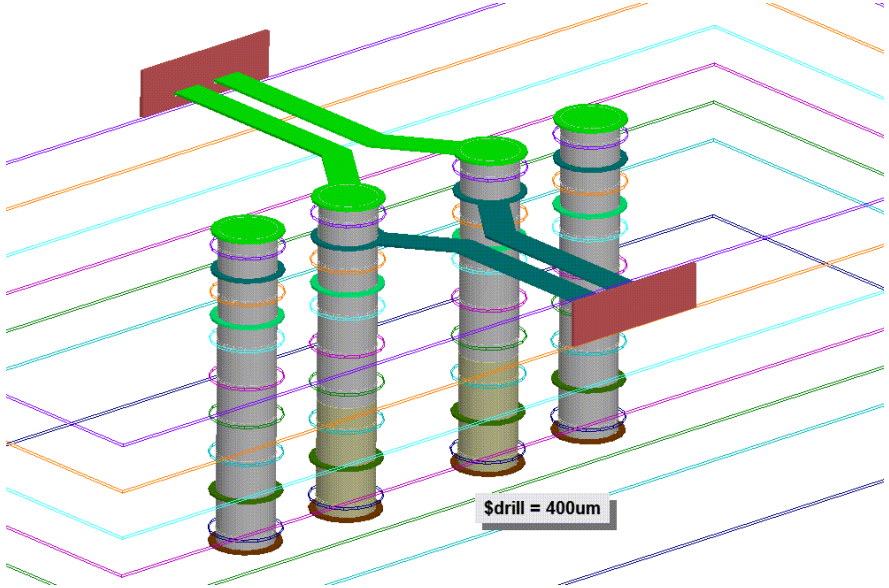
HFSS 3D Layout

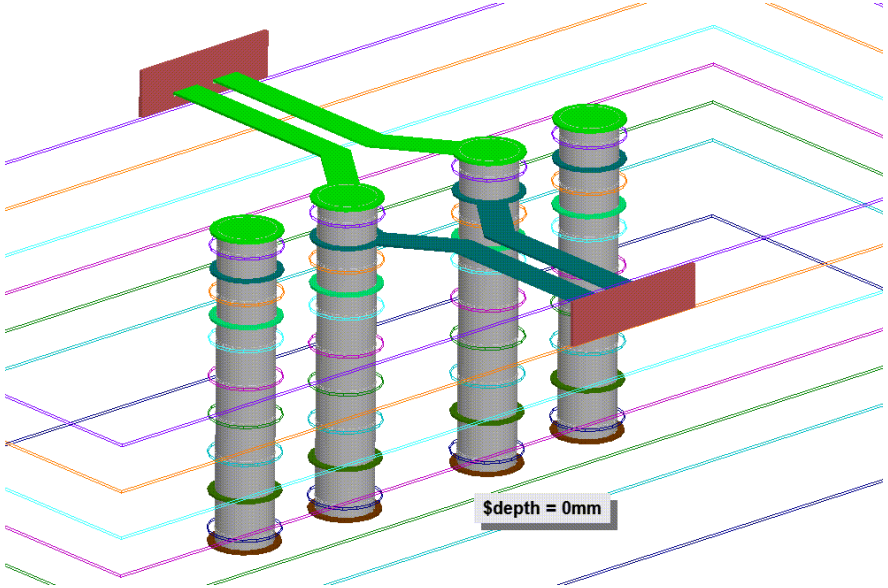
Arbitrary Backdrill Depth



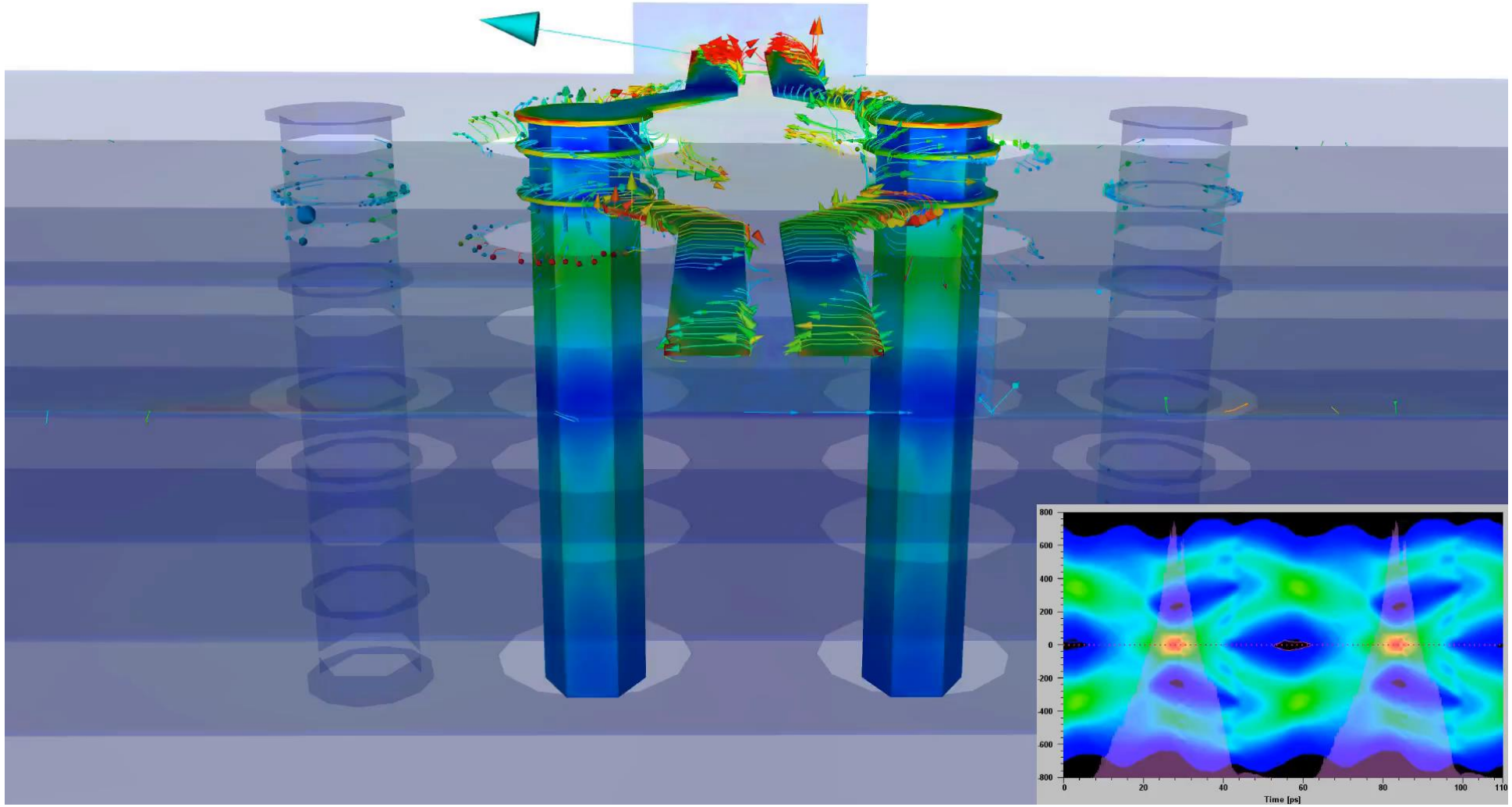
- Via stubs can create significant signal integrity disturbances. Backdrilling is a technique that removes these stubs and can be defined as:

  A. **By Depth**: a user-specified length from above the top of the stackup and/or below the bottom of the stackup
  B. **By Layer with an offset**: The backdrill will reach to the specified distance offset on the layer from above or below
  C. **By Layer (with no offset):**a user-selected layer is chosen from a drop-down menu. The backdrill will reach it from or below layer





Effects of Backdrill on 18GBPS Signal

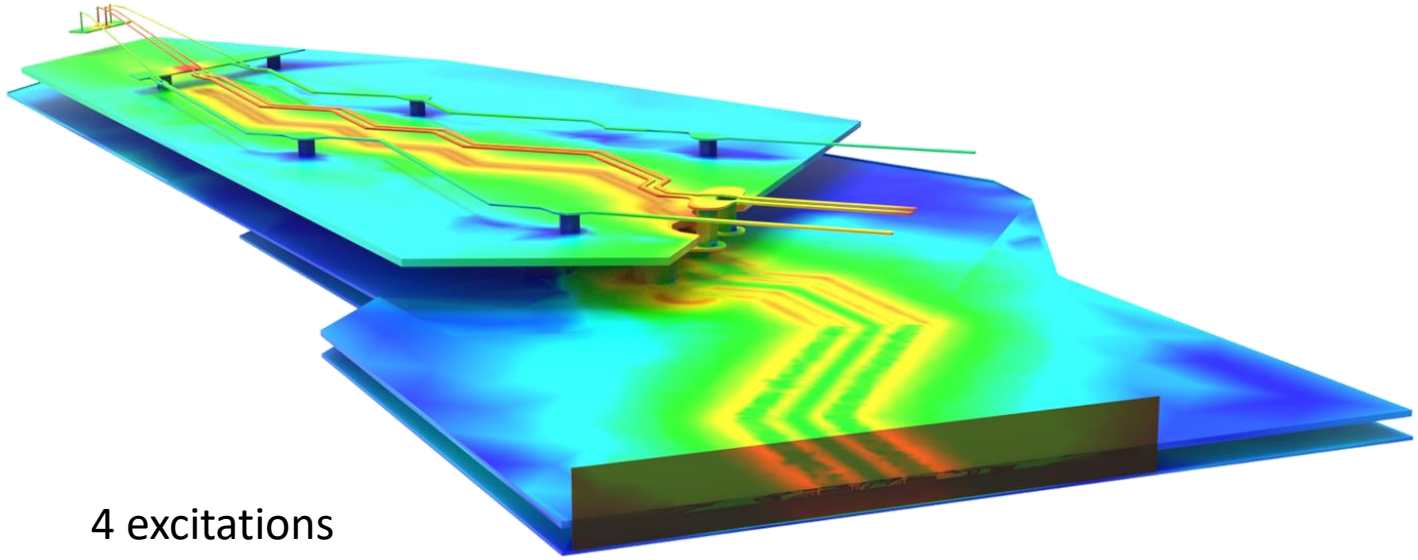


Waveport for Broadband Fast sweep in HFSS 3D Layout [Beta]

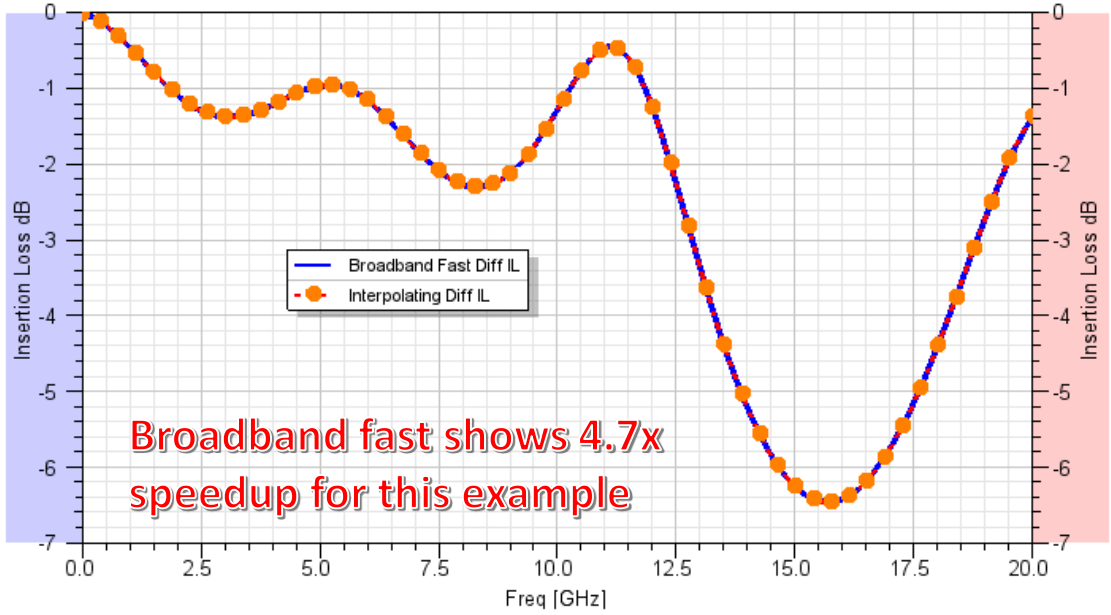
- Improved low frequency stability and performance
- Improvements to port Z0 extrapolation

Package on PCB (cutout) example

32 cores – Frequency sweep	
Interpolating	Broadband fast
00:15:02	00:03:10

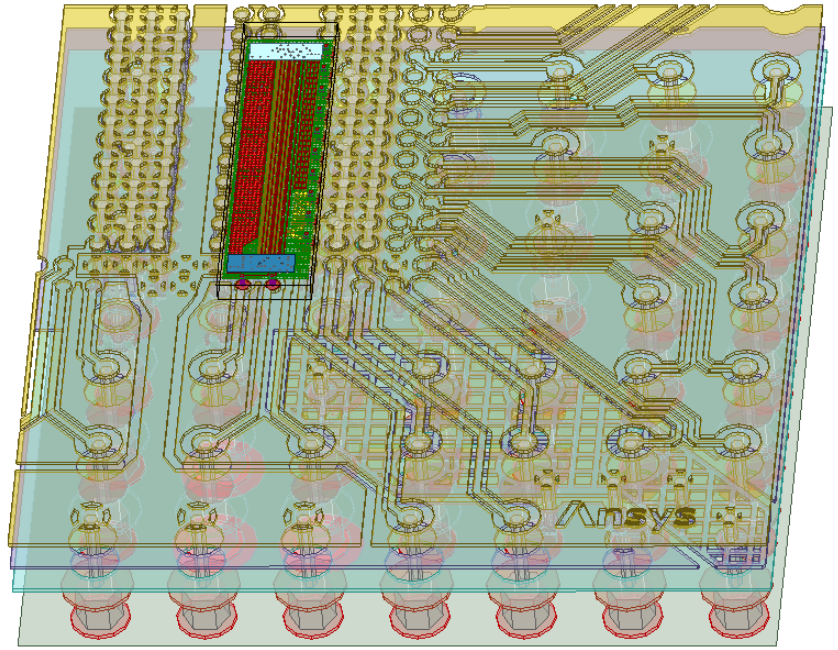


4 excitations



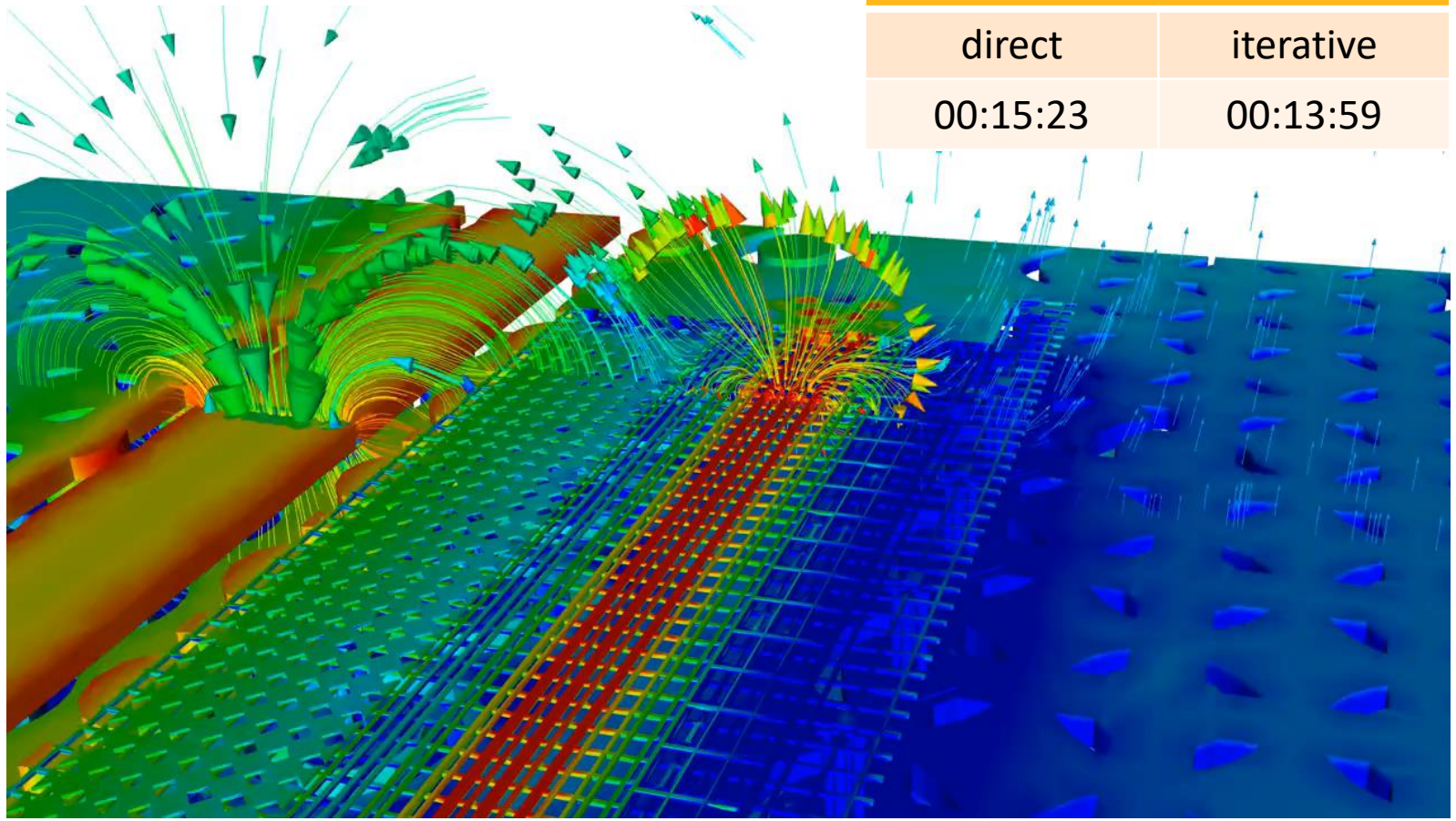
Iterative Solver Option for Mesh Fusion in HFSS 3D Layout

Interposer on package



6 excitations

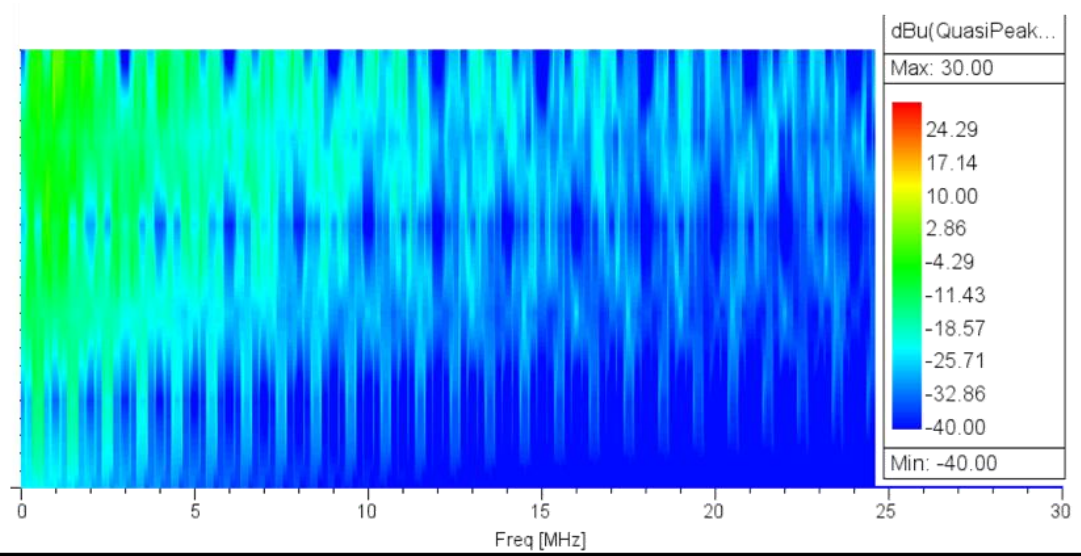
32 cores	
direct	iterative
00:15:23	00:13:59

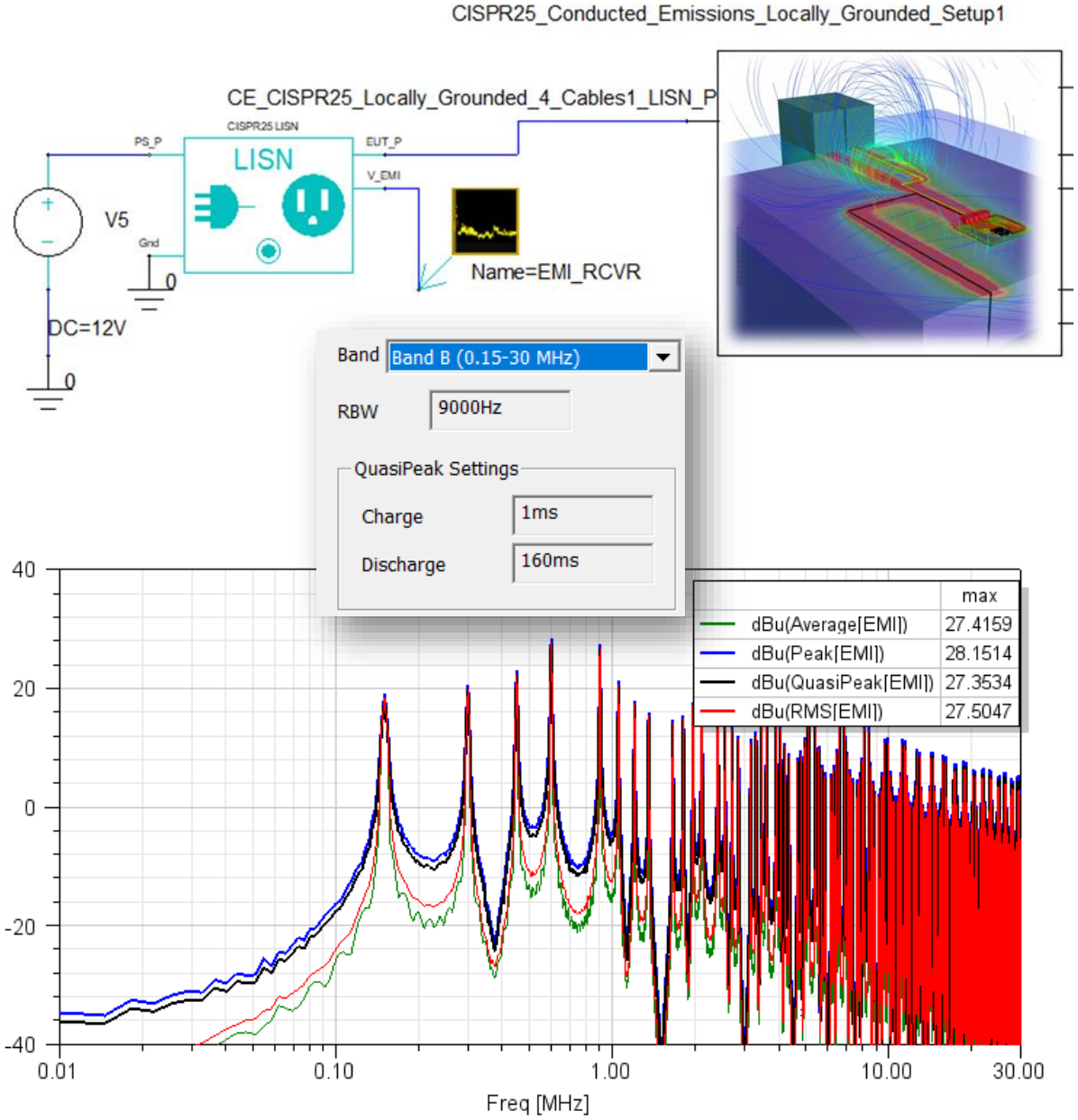


EMIT, Circuit, SPISim, and FilterSolutions

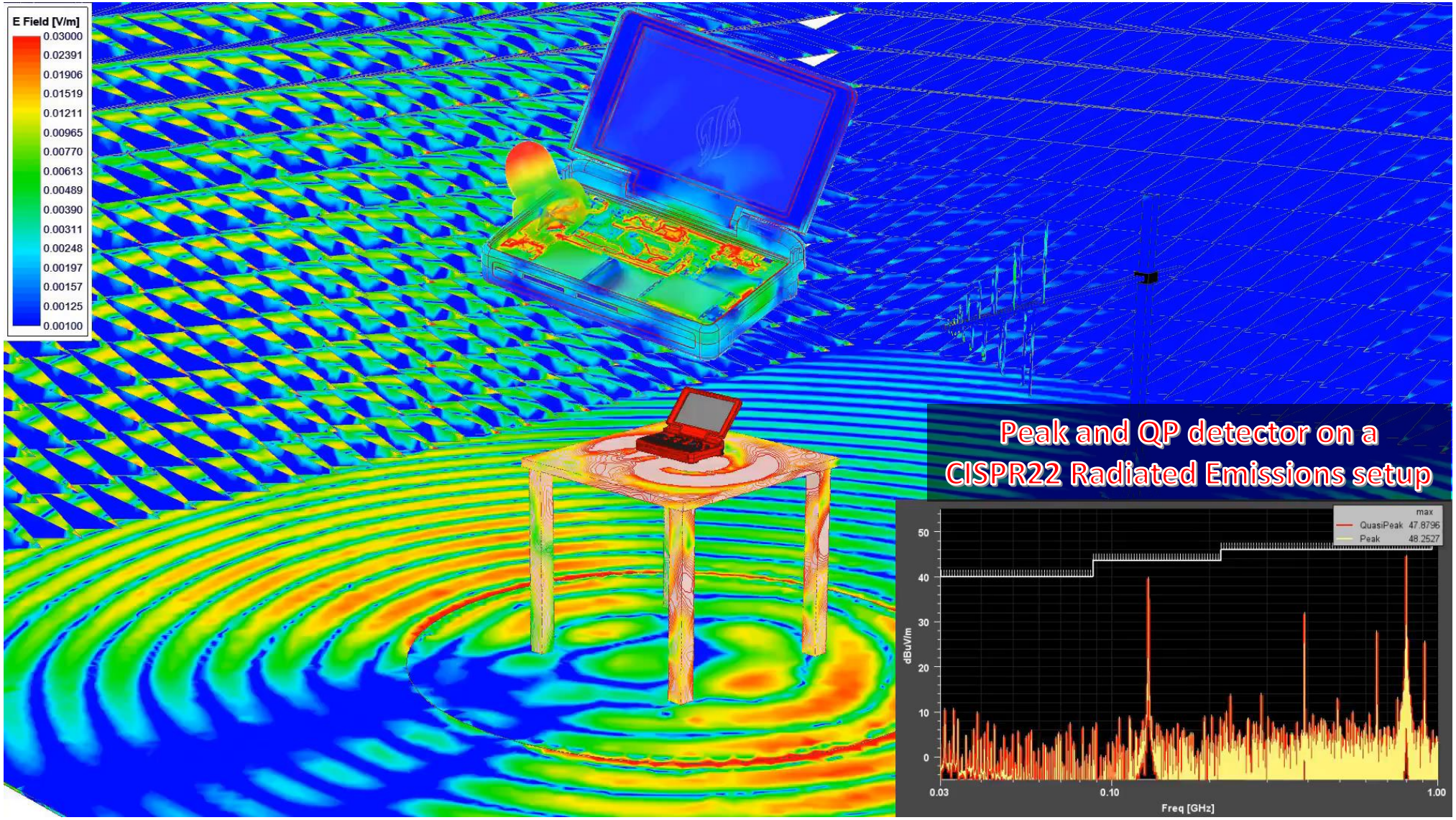
2023.1 – EMI Receiver [Beta]

- EMI Receiver
  - Transient signal undergoes a Short-Time-Fourier-Transform (STFT) analysis with Gaussian window
    - Outputs 3D spectrogram data
    - Displays frequency component change in the signal vs. time
  - Spectrogram data is passed through desired EMI detectors to obtain emissions in the selected freq. range
  - Supports CISPR16-1-1 Band A to D with Peak, QuasiPeak, Average and RMS Detections.





2023.1 – EMI Receiver [Beta]

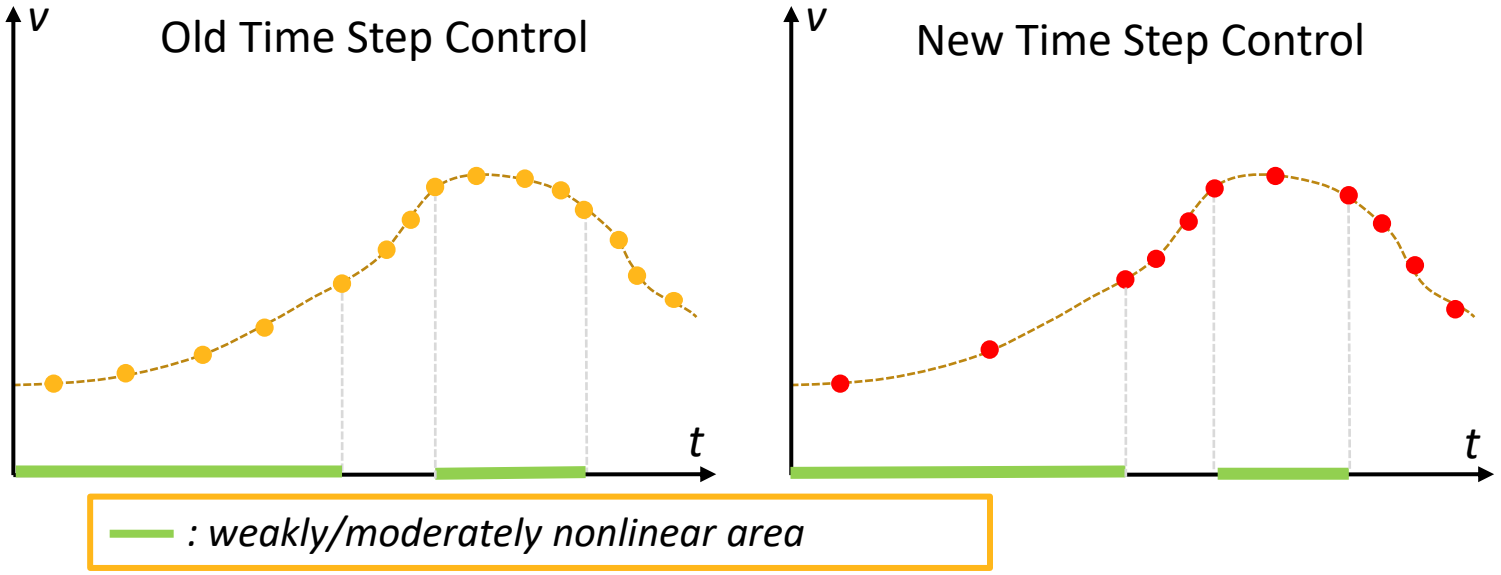


2023.1 – Adaptive time stepping improvements

Motivation:
- Small time step can improve the chance of convergence
- Small time step slows down simulation
- Use larger time step without loss of accuracy and convergency when applicable

Solution:
- Keep the philosophy of the existing multi-stage time step control algorithm
- Use the number of Newton iterations as an indicator of nonlinearity
- Increase time step for weak/moderate nonlinearity regimes

Impact:
- Reduce the total number of time steps and Newton iterations, improve simulation time

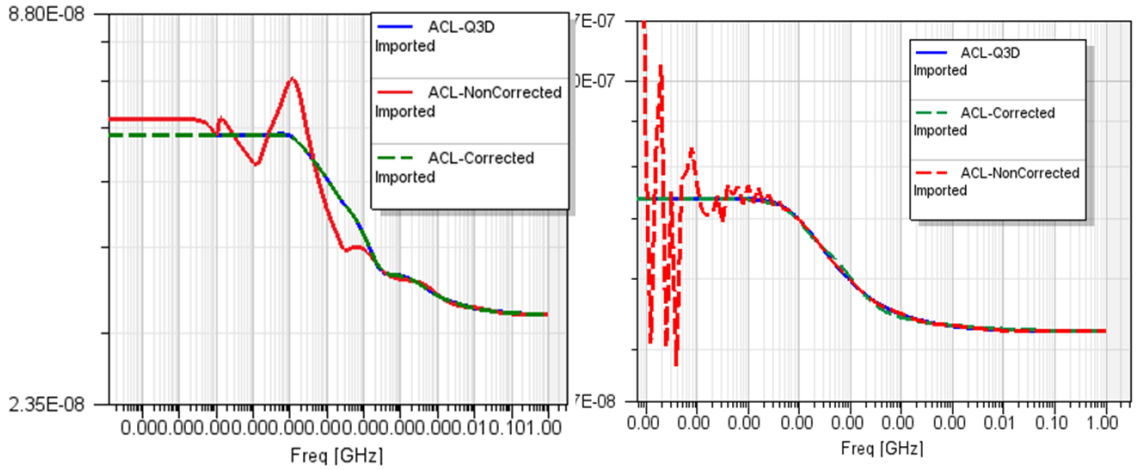


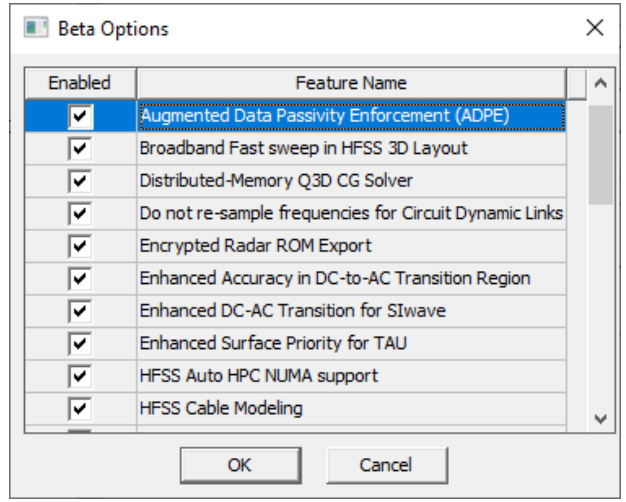
	Two-stage LTE Adaptivity			Two-stage LTE & nonlinearity Adaptivity			Impr. in Newton step (%)	Impr. in Sim. time (%)
h	# time step	Avg. Newton	cpu time(s)	# time step	Avg. Newton	cpu time(s)		
1e-9	9.90e+02	3.8	0.233	9.48e+02	3.9	0.223	4.24	4.29
1e-11	7.41e+04	2	7.18	6.69e+04	2	6.702	9.72	6.66
1e-13	7.39e+06	2	718.997	6.68e+06	2	658.687	9.61	8.39

State Space Fitting Enhancements

- Improvements to Q3D RLGC Spice export
  - For new AC-to-DC transitions region Q3D solver, algorithm developed to enforce stability and automatically perform causal correction

- New Augmented Data Passivity Enforcement
  - ADPE: State-space fitting option that helps with passivity enforcement for under-sampled data
  - Improves the use of Tsuk-White Algorithm (TWA) interpolation and passivity enforcement when basis points are under-sampled





AMI Support for DDR5 asymmetric rising/falling edges

Motivation:

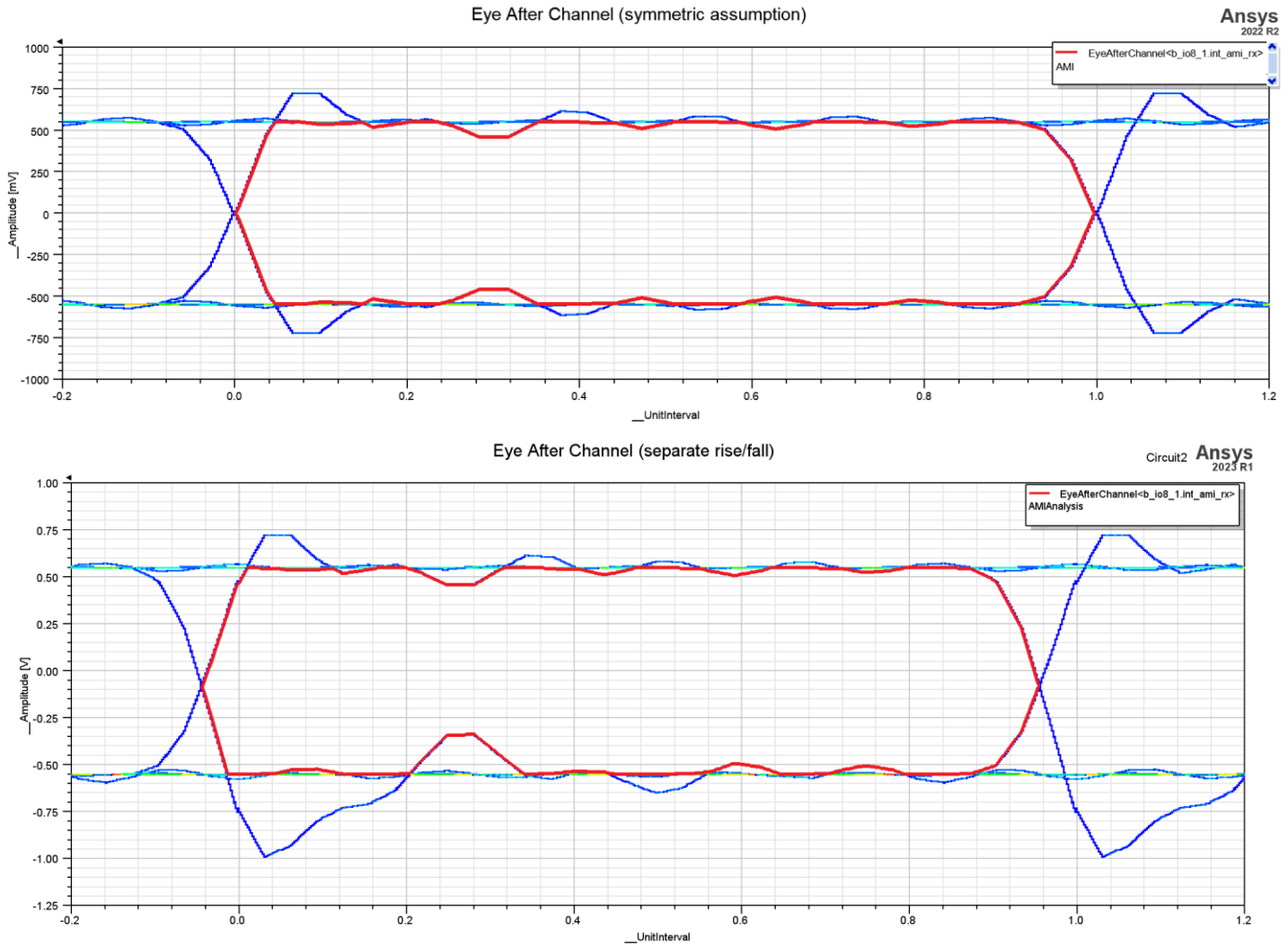
- AMI was originally developed for SerDes applications
- Channel and IBIS model driving the step response assumed LTI
- A step (impulse) response characterized the entire channel.

Issue:

- AMI simulations are now used for DDR5 devices
- DQ channels are single-ended
- AMI model makers provide IBIS models that include different rising and falling edges times

Solution:

- For single-ended applications, AMI analysis no longer assumes a single step (impulse) response
- Channel output is based on convolving with different rising/falling responses
- Results available for asymmetric signals (e.g., DDR5 DQ)

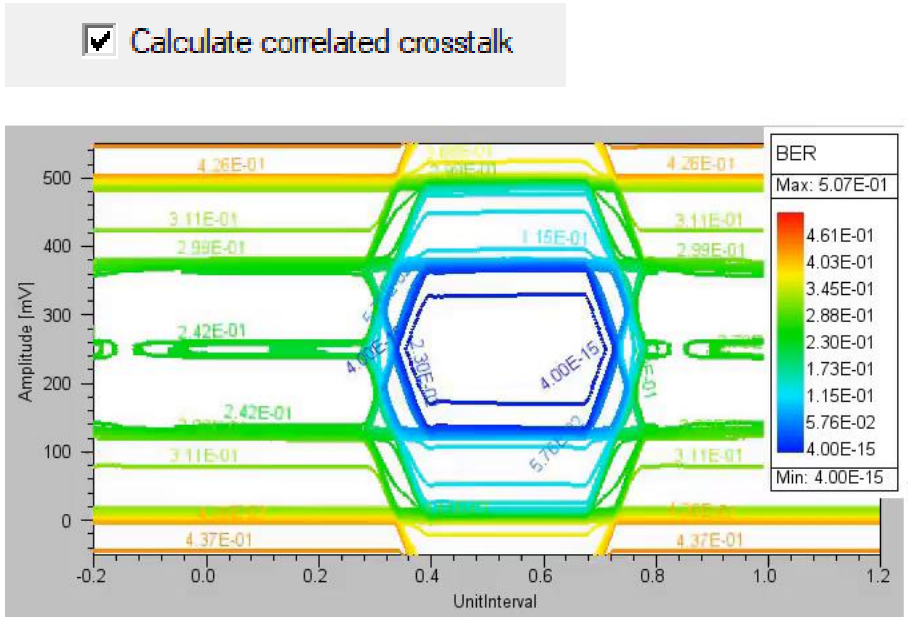


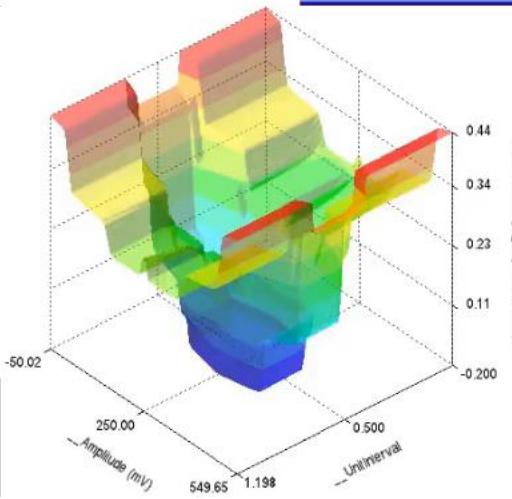
Correlated crosstalk option for VerifEye

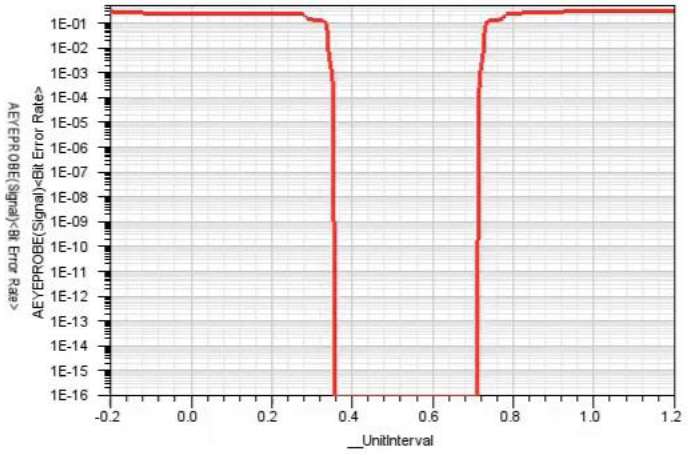
- Correlated crosstalk preserves the delays (i.e. jitter) between victim and aggressor lanes

- Uncorrelated crosstalk simulates the effects of crosstalk energy that can occur anywhere in the victim's eye diagram with equal probability

Correlated crosstalk VerifEye analysis of two parallel traces







Calculate ERL w/o using COM flow

Motivation:

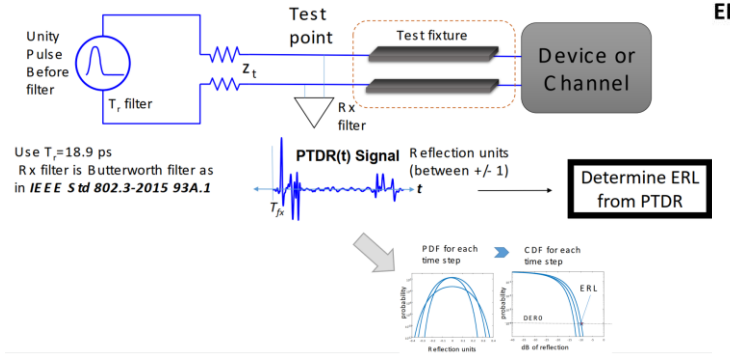
- SPISim's COM provides ERL calculation, but requires a config. settings which has 100+ input parameters
- Goal: Calculate ERL directly without going through COM

Solution:

- ERL menu item has been added in the for direct access
- Batch mode and UDO/UDS based approaches implemented to support direct ERL calculation

Impact:

- User can import multiple .snp file(s) and calculate their ERL values in GUI or batch mode
- HFSS 3D Layout/Circuit users now can optimize their design based on ERL results

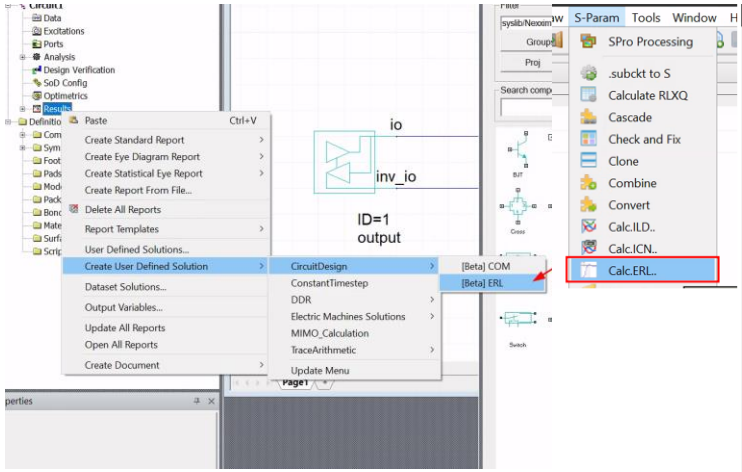


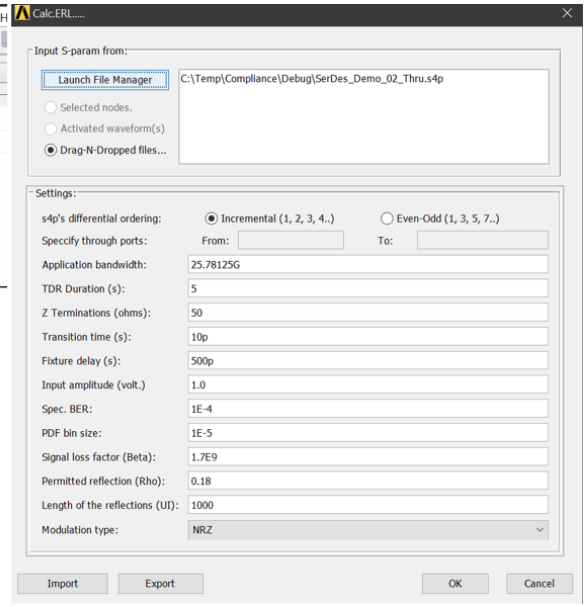
ERL: Effective Return Loss using PTDR

ERL Computation Parameters

- N_{bx} is the number for DFE taps or set by referencing clause
- T_b is the time for one symbol (aka UI) in ns
- t is time in ns
- T_{fx} is the time in ns associated with the end of the test fixture
- β_x is loss/ratio per unit time derived from the reference package loss in GHz
- ρ_x is the permitted reflection from the "missing side" of the channel
  - ρ_x is a reflection ratio and thus unitless

$$R_{eff}(t) = PTDR(t) \underbrace{\left(\rho_x(1+\rho_x)e^{\frac{\left(\frac{t-T_{fx}}{T_b}-(N_{bx}+1)\right)^2}{(N_{bx}+1)^2}}\right)}_{\text{DFE re-reflection compensation}} \underbrace{10^{\frac{\beta_x\left(t-T_{fx}-T_b(N_{bx}+1)\right)}{20}}}_{\text{Package Loss compensation}}$$





SPISim: New SERDES Compliance checks

Motivation:

- AEDT/HSFSS users perform compliance check for SERDES standards/specs
- Specs. have input data comprised of various sections, automatic “cascading” available during process

Solution:

- SPISim’s compliance check to support eight additional industry standards
- “Cascaded” .snp files automatically for various aspect of compliance checking
- SPISim GUI mode and batch supported
- Includes TDR report for additional design performance metrices

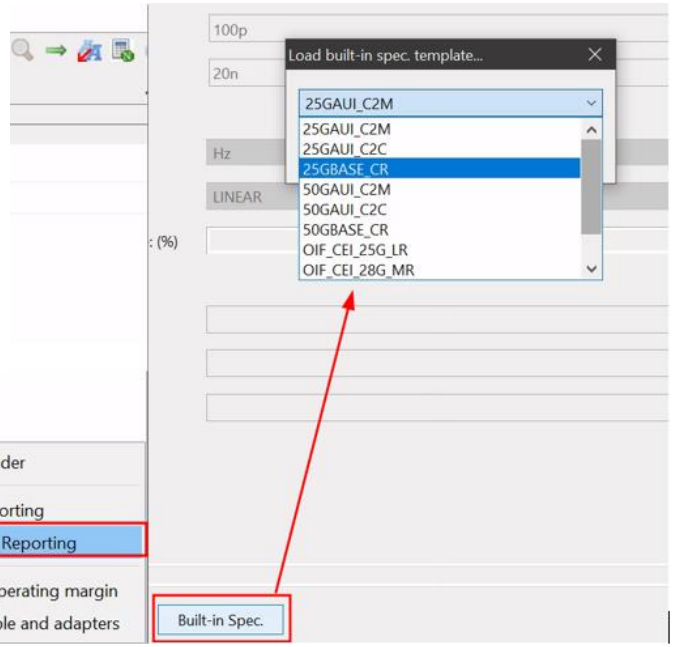
Impact:

- AEDT/HFSS users can perform compliance checks for .snp files within the Ansys environment/toolsets

[25GAUI C2M (802.3by-2016, Annex 109B)]
[25GAUI C2C (802.3by-2016, Annex 109A)]
[25GBASE-CR (802.3by-2016, Annex 110A)]

[50GAUI-1 C2M (802.3cd-2018, Annex 135G)]
[50GAUI-1 C2C (802.3cd-2018, Annex 135F)]
[50GBASE-CR (802.3cd-2018, Annex 136A)]

[CEI-25-LR (OIF-CEI-4.0, Chapter 11)]
[CEI-56G-LR-PAM4 (OIF-CEI-4.0, Chapter 21)]



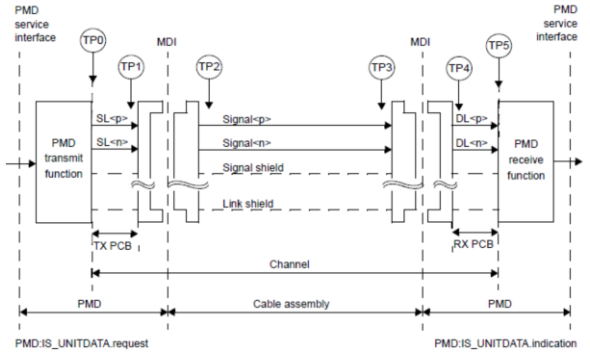
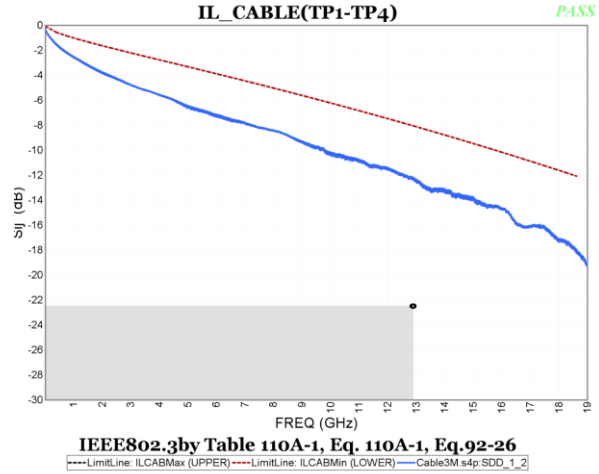
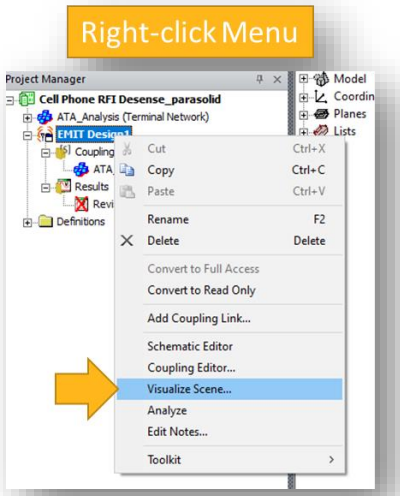


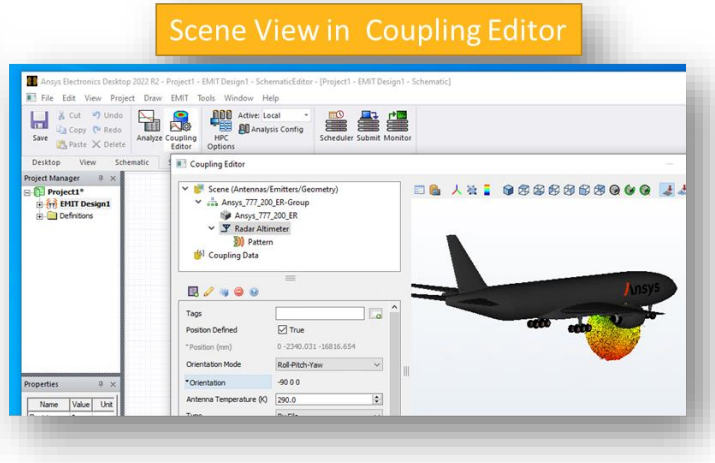
Figure 110–2—25GBASE-CR or 25GBASE-CR-S link (one direction is illustrated)

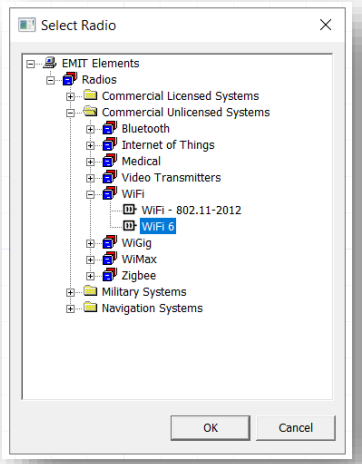


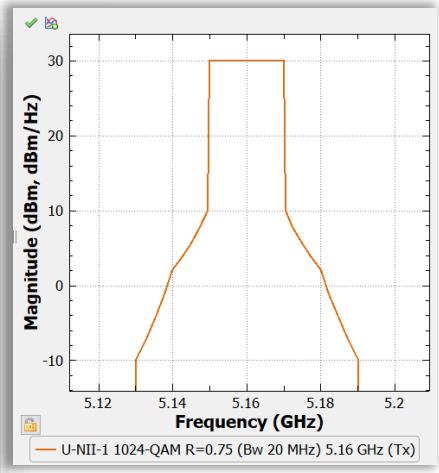
EMIT usability enhancements and new radio models

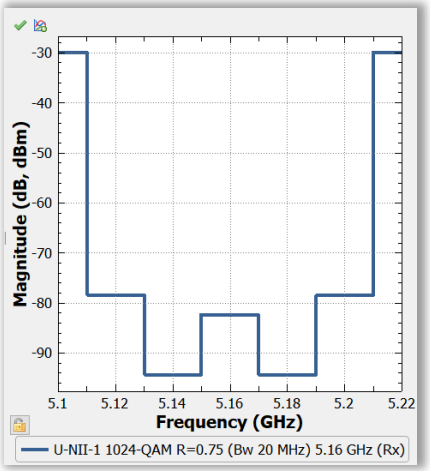
- Usability enhancements
  - Added "visualize scene" action
  - User setting for coupling dialog on link
  - Show “Add Coupling Link" dialog upon adding EMIT design
  - Show Touchstone port names for port assignment
  - Double-click to select radio/emitter in library dialog
  - EMIT classic is no longer part of the install starting on 2023 R1
- New WiFi 6 transceiver model





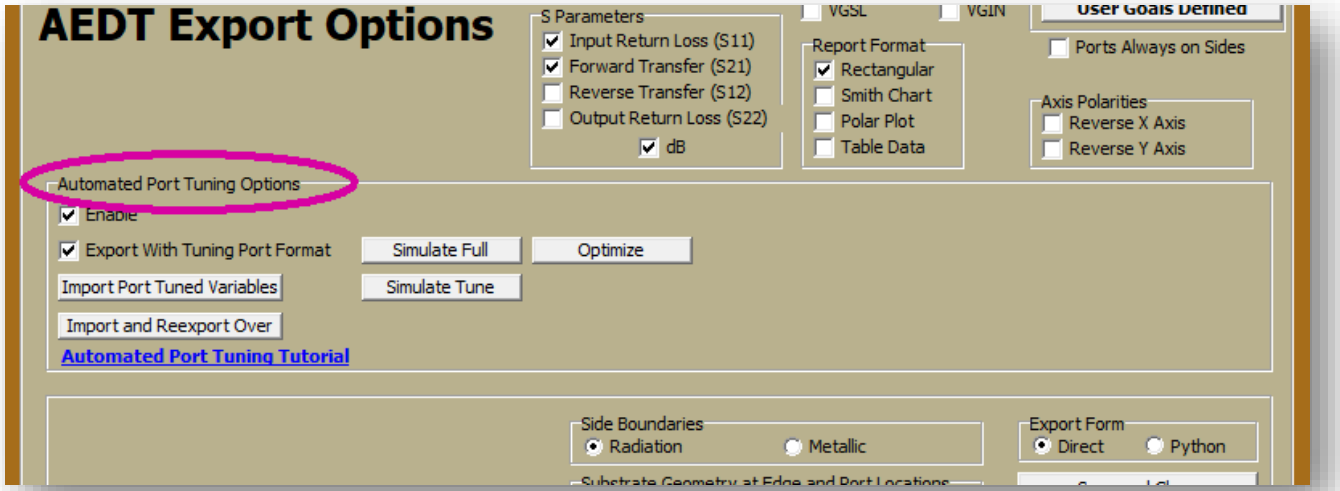






FilterSolutions: HFSS 3D Layout Automatic Port Tuning

- Simulation, optimization, and design reconstruction controls provided for in FilterSolutions desktop export panel.
  - Export the design in tuning schematic and HFSS co-simulation format
  - Simulate with Circuits and HFSS co-simulation
  - Import the optimized variables and reconstruct the filter
  - Repeat as needed until optimization is satisfactory.



AEDT Desktop and Core

Ansys Electronics Desktop

- Parasolid kernel for 3D Modeler
  - Official migration to Parasolid modeling kernel

- Auto multi-level distribution for LSDSO
  - Each distributed process automatically determines best allocation of available cores
    - frequency point distribution, solver distribution, etc…

- Native non-graphical image export
  - ExportModelImageToFile script command works in graphical and -ng mode on both Windows & Linux


Ansys