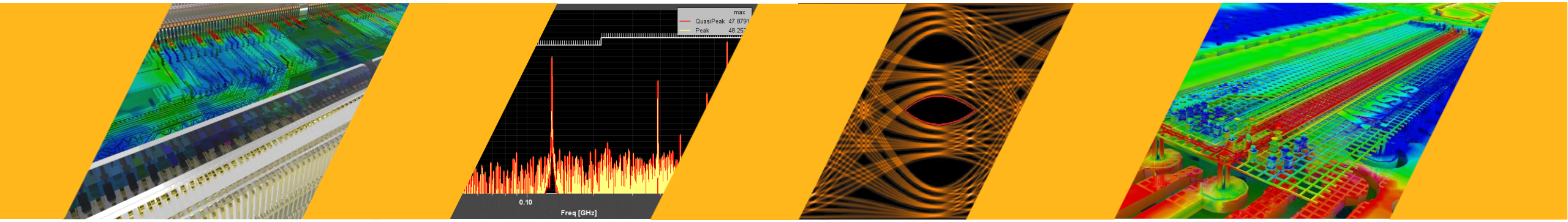
Release 2023 R1 Highlights
Signal and Power Integrity

Ansys HFSS, SIwave, Q3D, HF Circuit

Ansys signal and power integrity 2023 R1 highlights



- ✓ Improved **workflows for layout component in HFSS 3D**
- ✓ **Arbitrary backdrill** depth in HFSS 3D Layout
- ✓ **Waveport support and enhancements for Brodaband Fast sweep** in HFSS 3D Layout
- ✓ **New DC IR plot features, validation check optimizations** and **HFSS regions enhancements** for SIwave
- ✓ Support for **asymmetrical rise/fall times** for IBIS AMI models and new **COM workflow** in Circuits
- ✓ **Q3D distributed CG solver** and new enhanced **DC-to-AC transition region solver**

HFSS 3D

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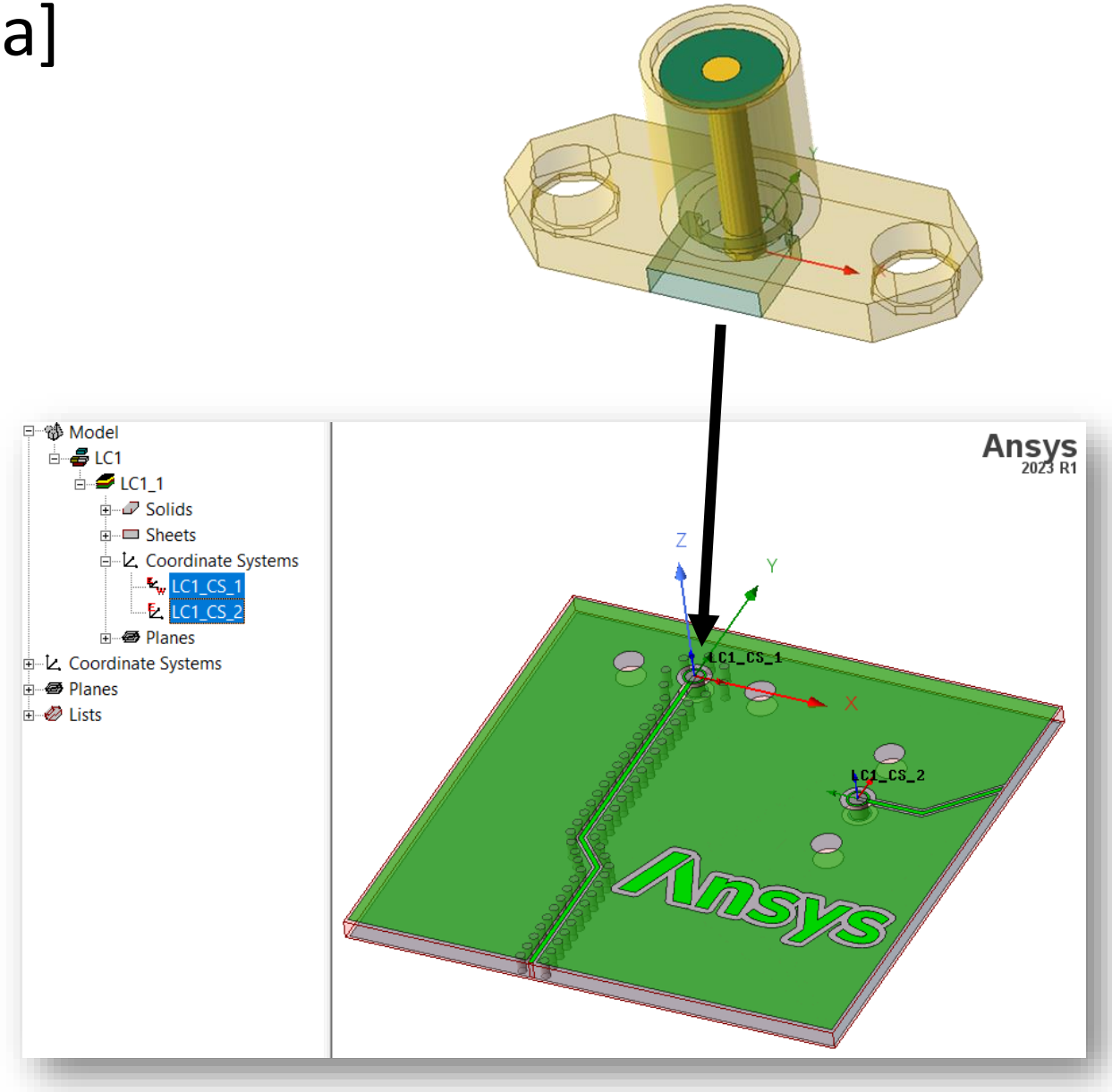
Layout component workflow [Beta]

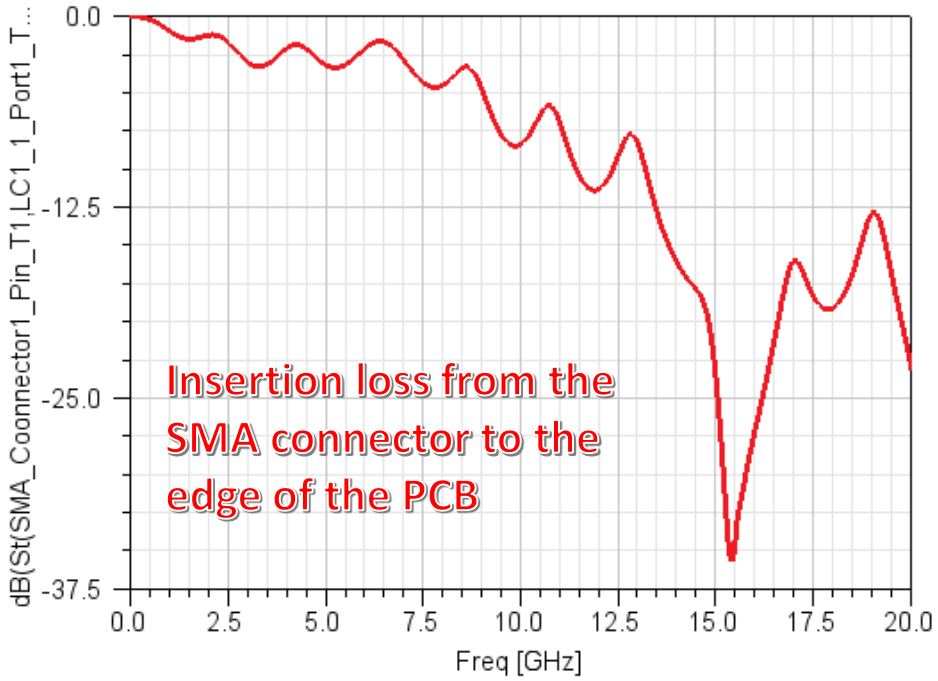
- New workflow for component placement
- Users can use reference coordinate systems defined in EDB in HFSS
  - Easily place connectors on right locations
- Supports mesh fusion
- Layout component's bounding box and ports are actual geometry. Rest of the layout is only for visualization
- Allow editing the layout component definition right from HFSS
- Visualization settings can be set by stack up layers or individual nets

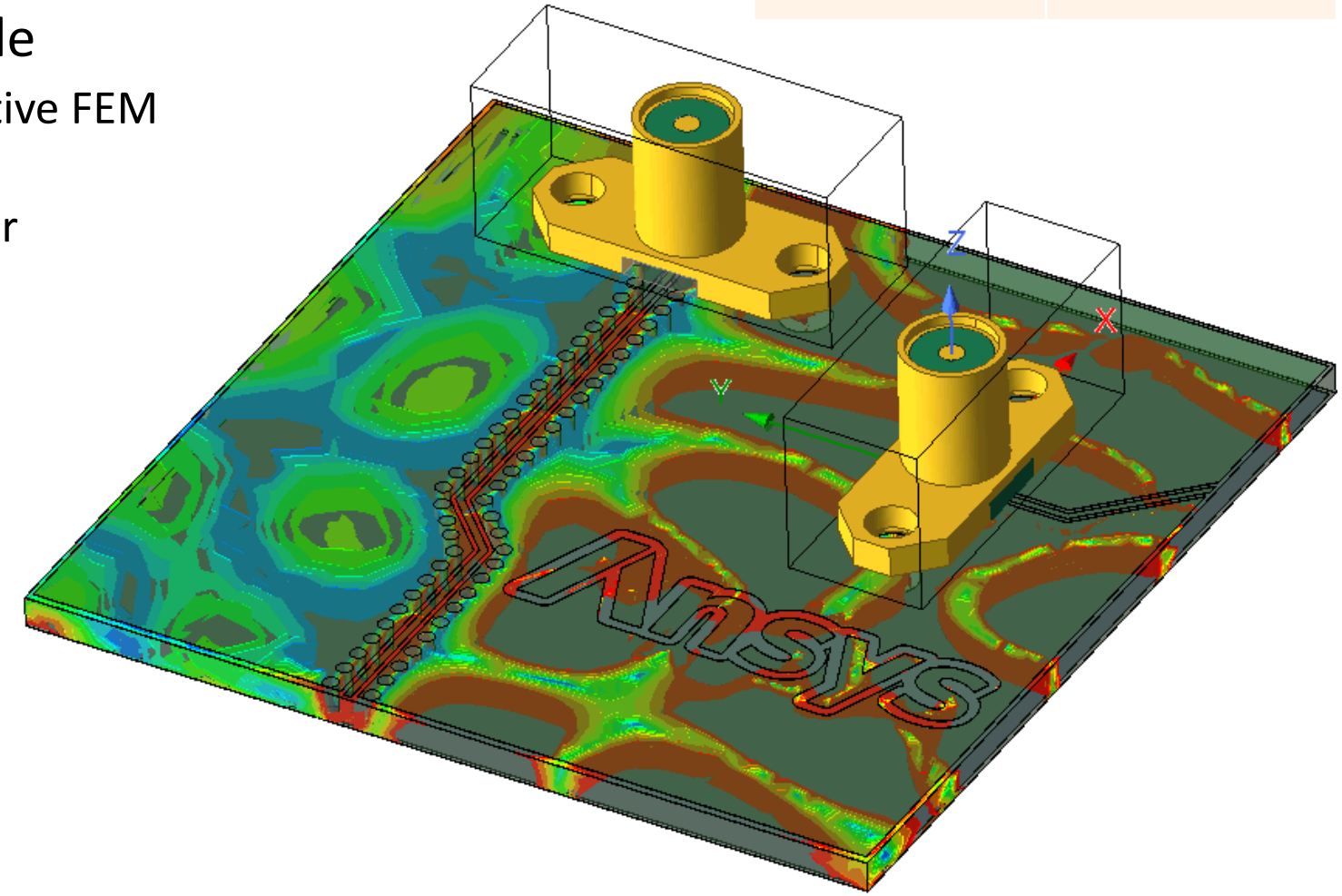


Layout component workflow [Beta]

32 cores	
Time	Max RAM
00:14:04	2.09 GB

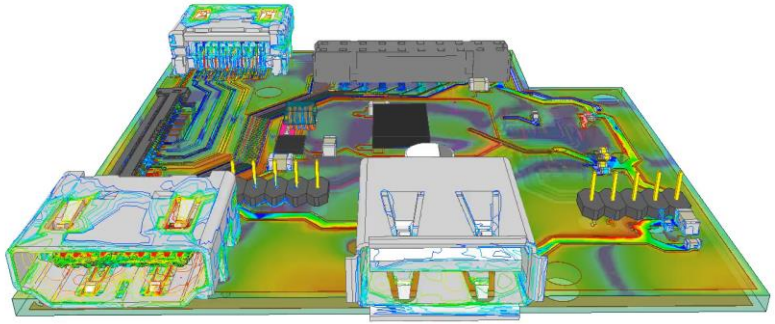
- SMA connector on board example
  - Mesh fusion with 3 domains plus native FEM
    - Layout component and 2 SMA connectors
  - Mesh fusion with <u>new</u> iterative solver





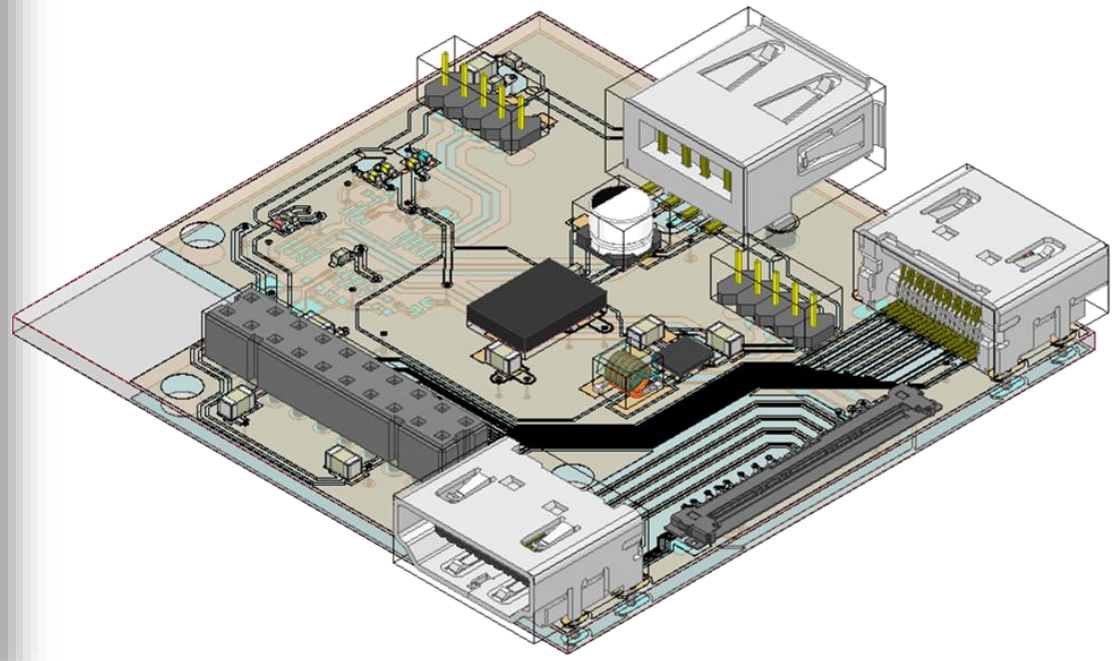
Layout component workflow [Beta]

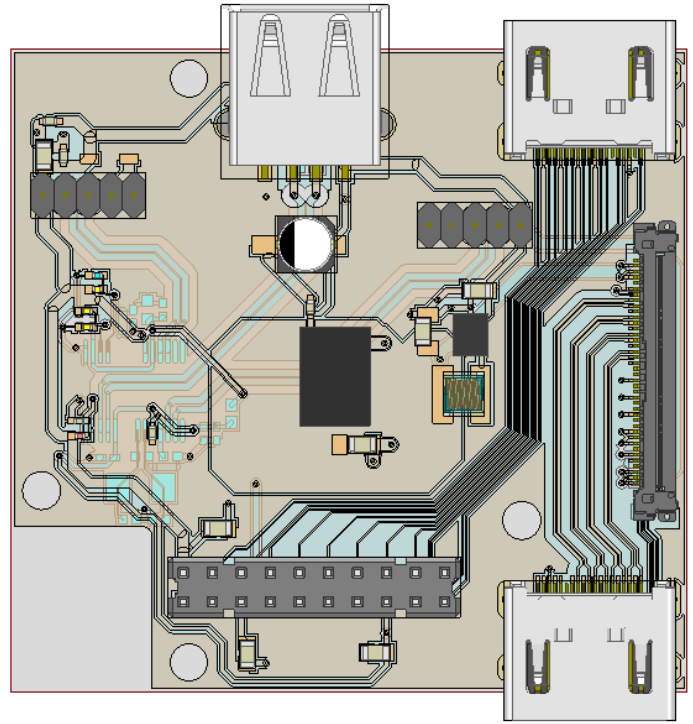
- Full PCB assembly
  - Mesh fusion with 29 domains plus native FEM



Mesh Fusion(Beta) Settings

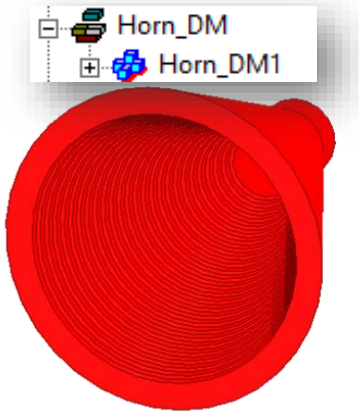
Component Name	Meshing Type	Enable
10x2_Connector1	Volume - Classic	☑
Bulk_Capacitor1	Volume - Classic	☑
Capacitor_1_1	Volume - Classic	☑
Capacitor_1_2	Volume - Classic	☑
Capacitor_1_3	Volume - Classic	☑
Capacitor_1_4	Volume - Classic	☑
Capacitor_1_5	Volume - Classic	☑
Capacitor_1_6	Volume - Classic	☑
Capacitor_1_7	Volume - Classic	☑
Capacitor_2_1	Volume - Classic	☑
Capacitor_2_2	Volume - Classic	☑
Capacitor_2_3	Volume - Classic	☑
Capacitor_2_4	Volume - Classic	☑
Capacitor_3_1	Volume - Classic	☑
HDMI_Connector1	Volume - Classic	☑
HDMI_Connector2	Volume - Classic	☑
Header5_Male1	Volume - Classic	☑
Header5_Male2	Volume - Classic	☑
Inductor1	Volume - Classic	☑
LC3_1	Volume - Phi	☑
Resistor_1_1	Volume - Classic	☑
Resistor_2_1	Volume - Classic	☑
Resistor_2_2	Volume - Classic	☑
Resistor_2_3	Volume - Classic	☑
Resistor_3_1	Volume - Classic	☑
Ribbon_Cable_Connector1	Volume - Classic	☑
U100_1	Volume - Classic	☑
U101_1	Volume - Classic	☑
USB_Connector1	Volume - Classic	☑



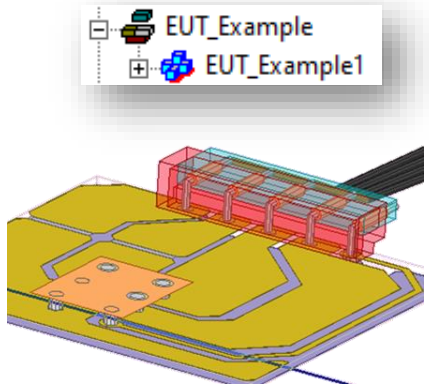


Modal Port in Terminal Design

- Allow both modal and terminal wave/lumped port in terminal solution type
- Allow both modal and terminal 3D components in a terminal solution type
- If there are modal ports in the design, edit source excitation switches to power

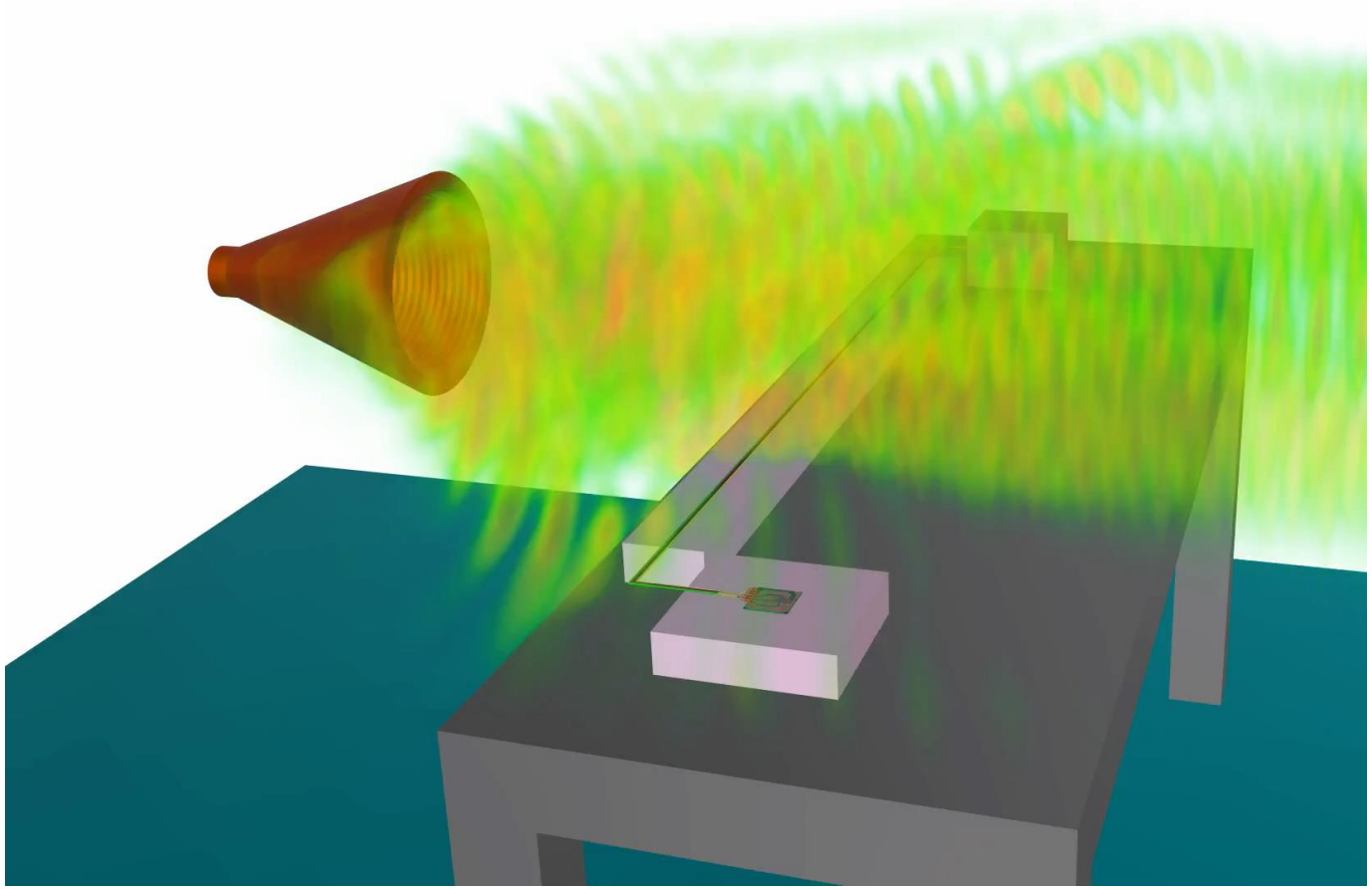


DM



DT

Radiated Immunity setup with Driven Modal and Driven Terminal components



HFSS 3D Layout

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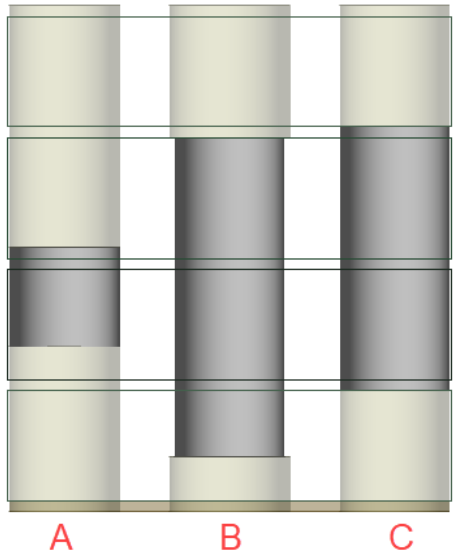
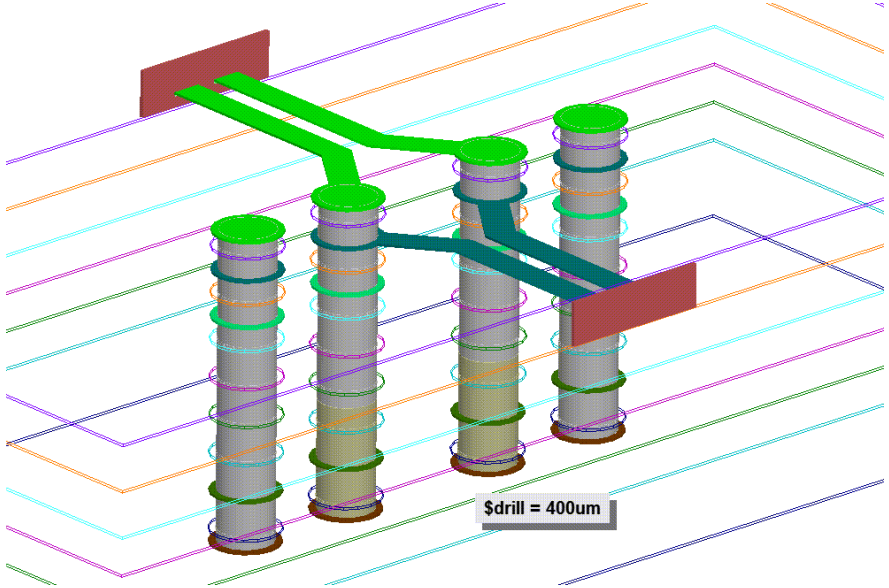
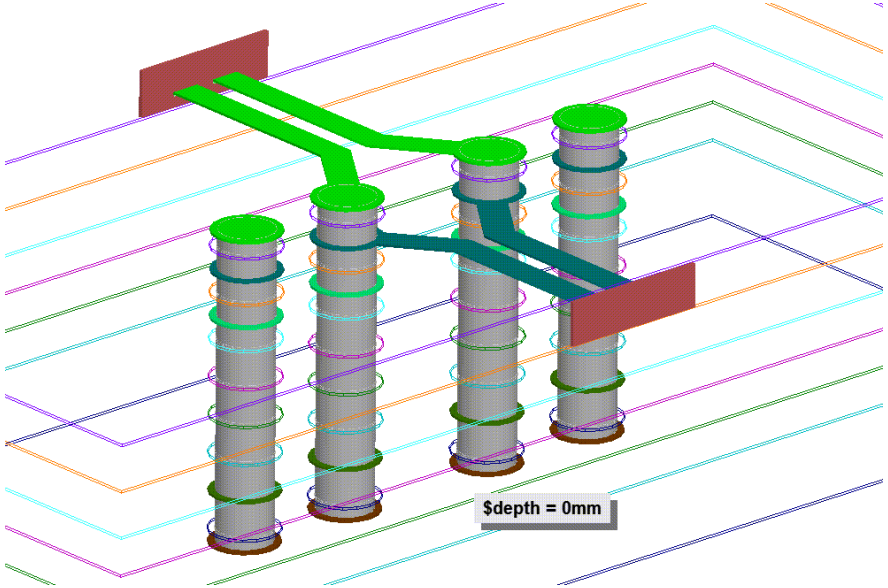
Arbitrary backdrill depth



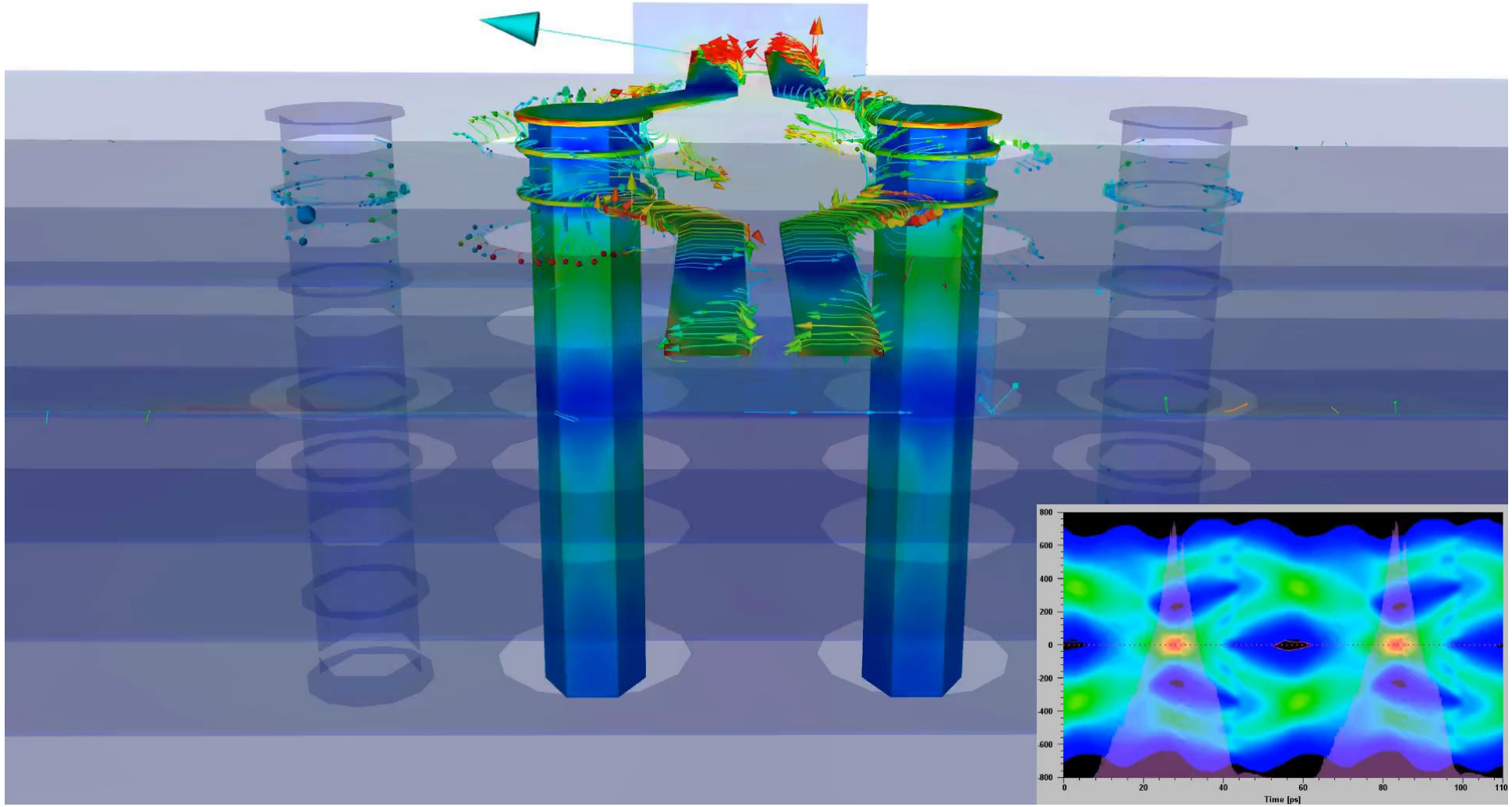
- Via stubs can create significant signal integrity disturbances. Backdrilling is a technique that removes these stubs and can be defined as:

  A. **By Depth**: a user-specified length from above the top of the stackup and/or below the bottom of the stackup
  B. **By Layer with an offset**: The backdrill will reach to the specified distance offset on the layer from above or below
  C. **By Layer (with no offset):**a user-selected layer is chosen from a drop-down menu. The backdrill will reach it from or below layer





Effects of backdrill on a 18GBPS signal

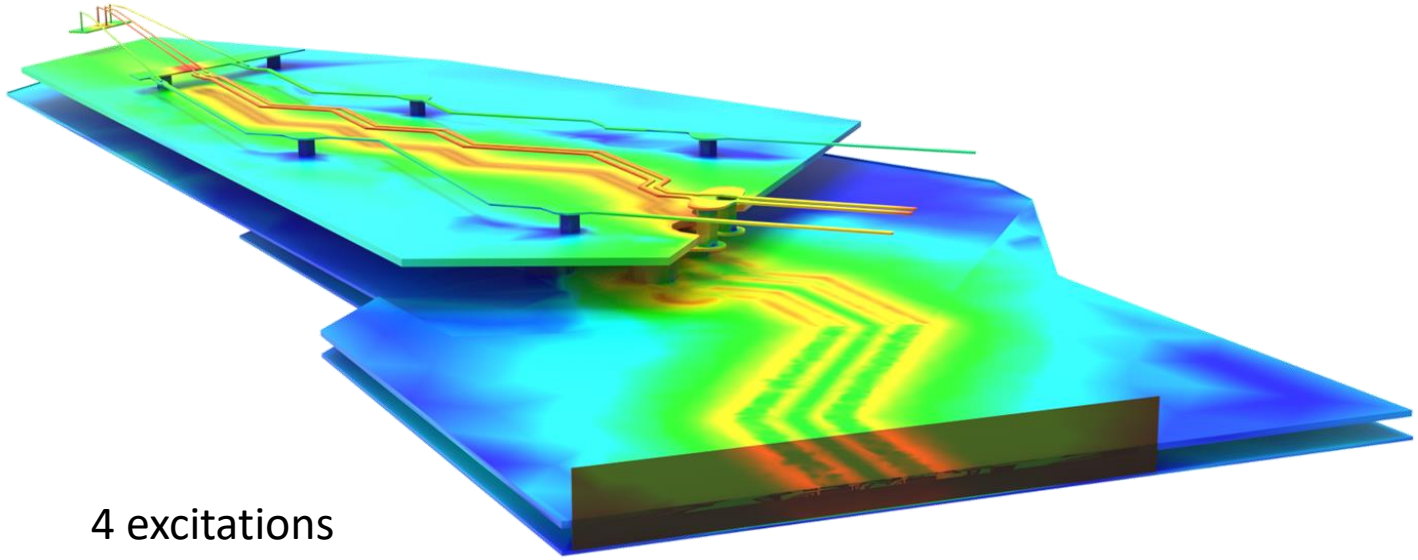


Waveport support for Broadband Fast sweep in 3DL [Beta]

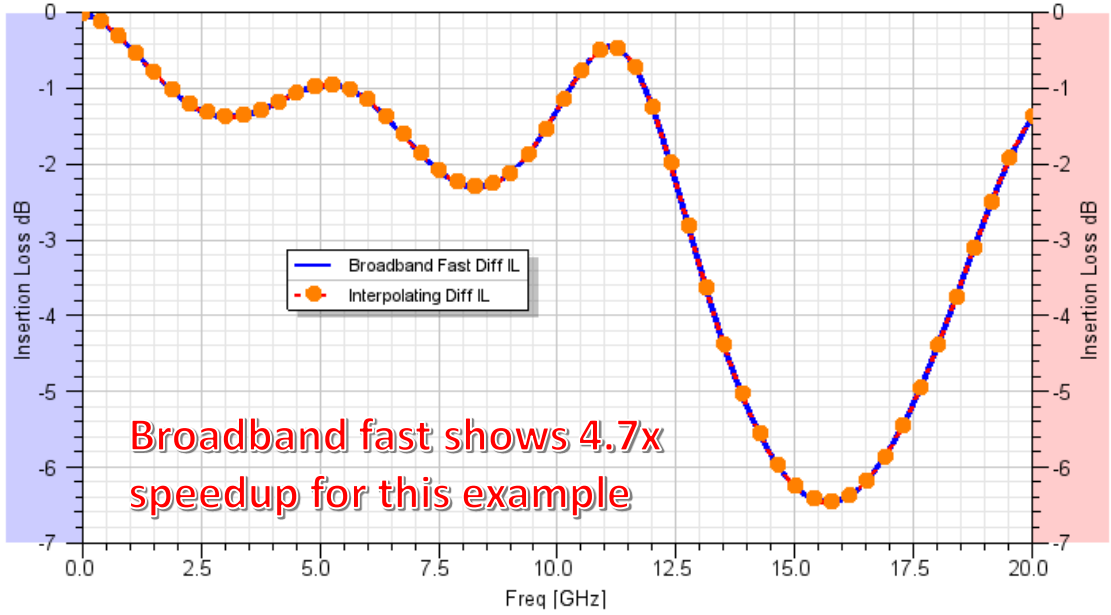
- Improved low frequency stability and performance
- Improvements to port Z0 extrapolation

Package on PCB (cutout) example

32 cores – Frequency sweep	
Interpolating	Broadband fast
00:15:02	00:03:10

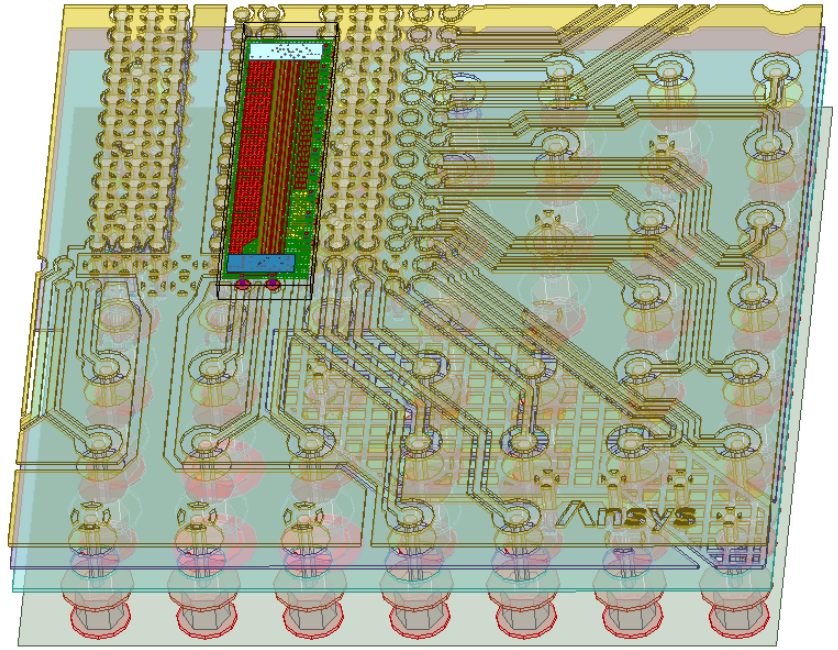


4 excitations



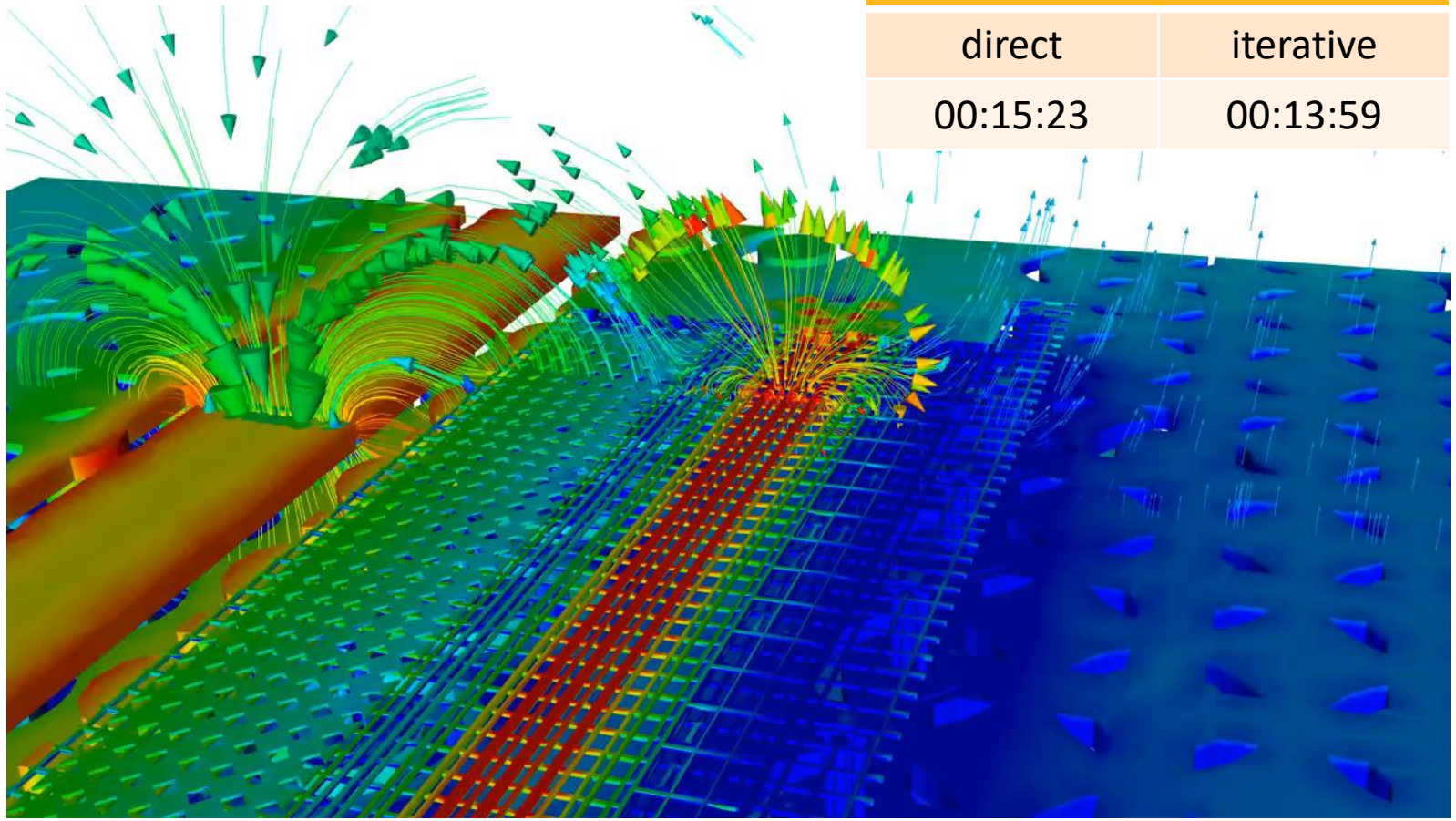
Iterative solver option for mesh fusion in HFSS 3D Layout

Interposer on package (cutout) example



6 excitations

32 cores	
direct	iterative
00:15:23	00:13:59

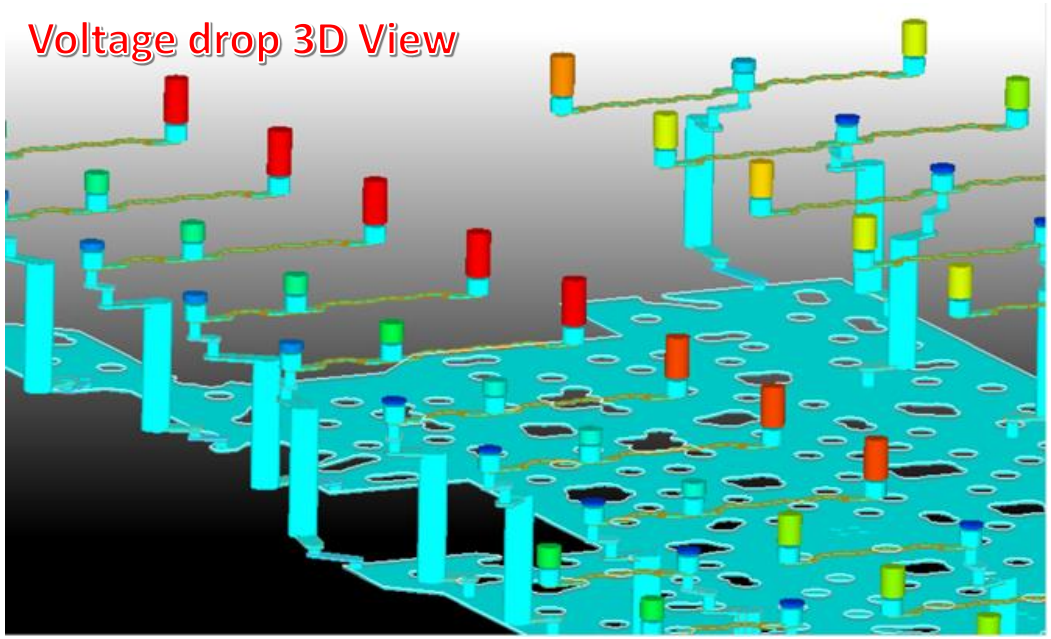


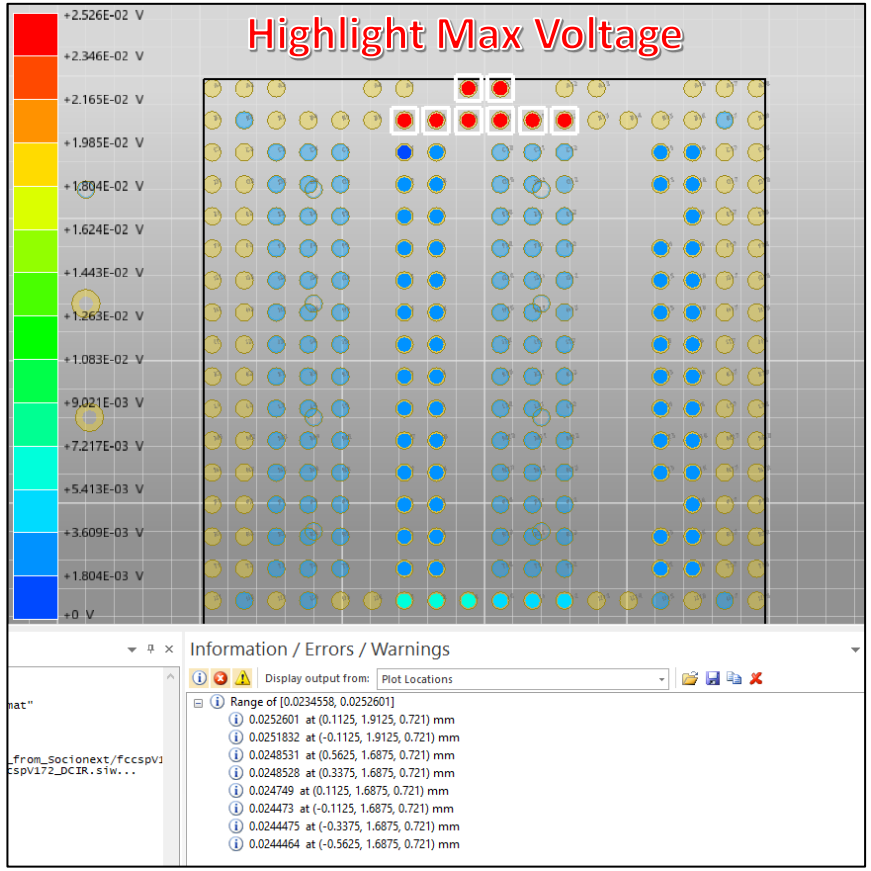
SIwave

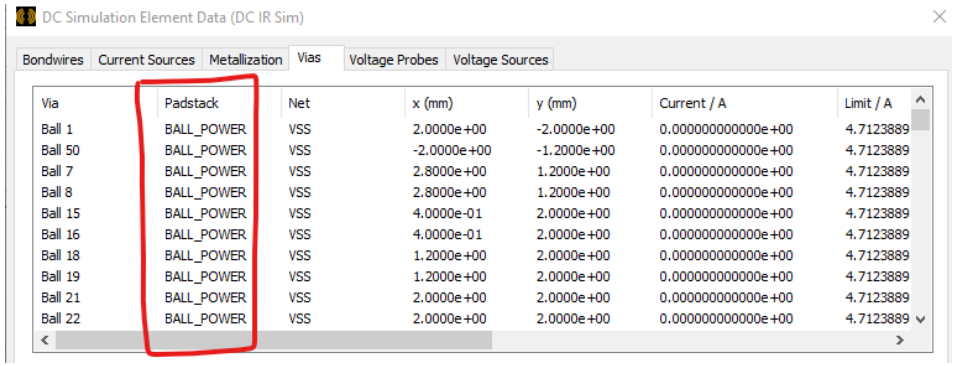
Ansys

DC IR post processing improvements

- 3D Voltage drop plot
  - Easier to visualize voltage drop hot spots
  - 3D plot view
- Highlight maximum voltage with white squares
- Add Padstack information in DC Element data report



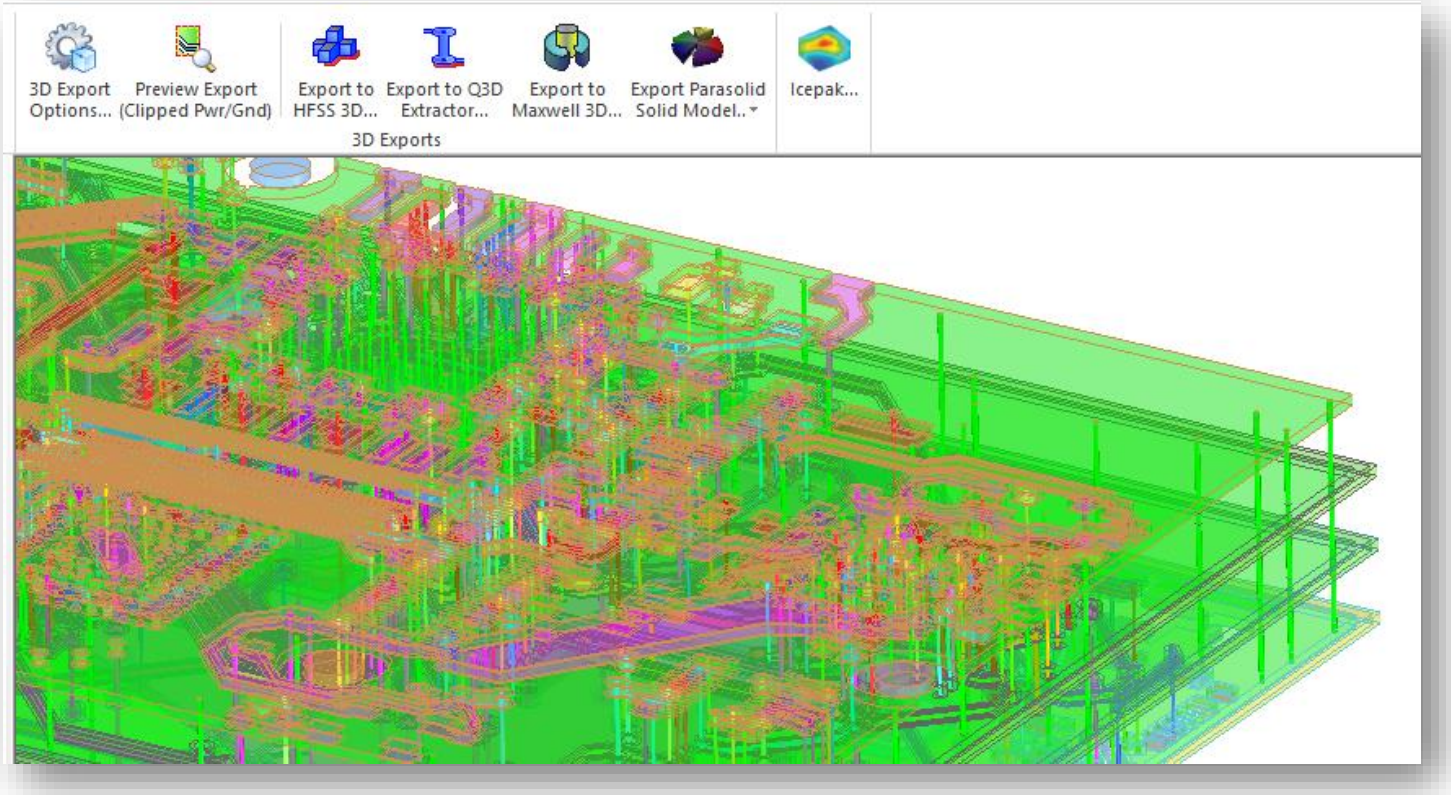


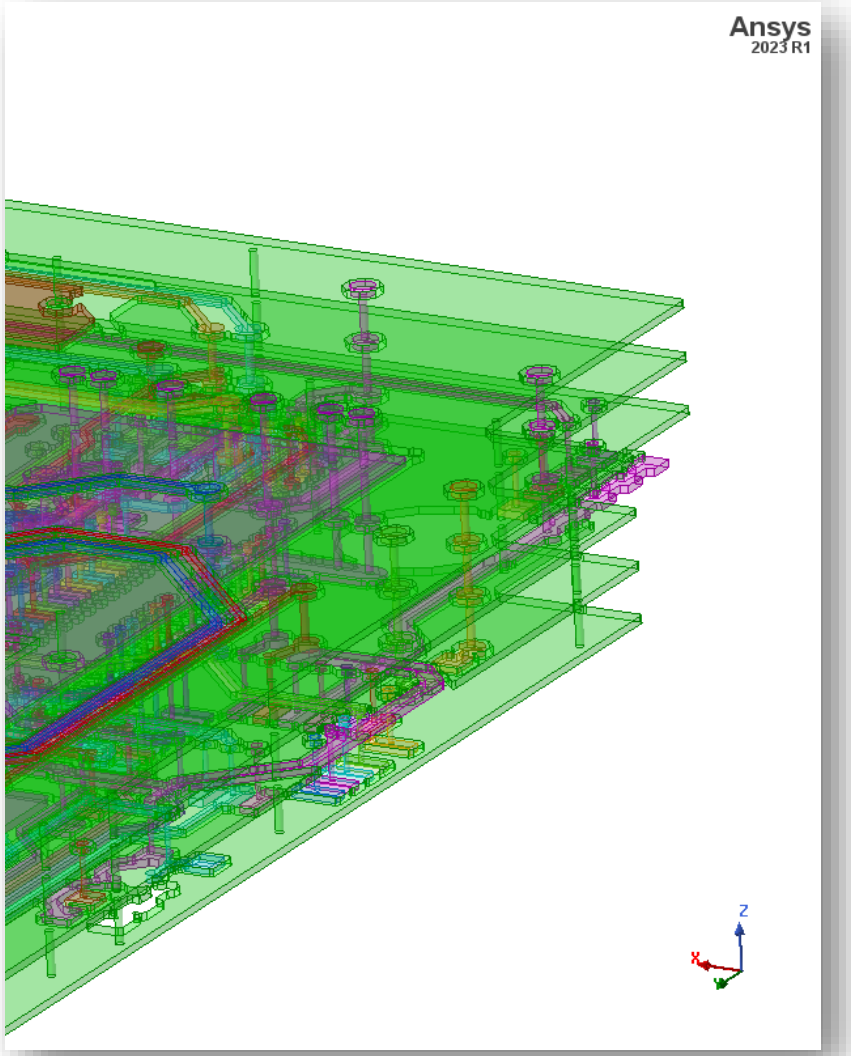


Via	Padstack	Net	x (mm)	y (mm)	Current / A	Limit / A
Ball 1	BALL_POWER	VSS	2.0000e+00	-2.0000e+00	0.000000000000e+00	4.7123889
Ball 50	BALL_POWER	VSS	-2.0000e+00	-1.2000e+00	0.000000000000e+00	4.7123889
Ball 7	BALL_POWER	VSS	2.8000e+00	1.2000e+00	0.000000000000e+00	4.7123889
Ball 8	BALL_POWER	VSS	2.8000e+00	1.2000e+00	0.000000000000e+00	4.7123889
Ball 15	BALL_POWER	VSS	4.0000e-01	2.0000e+00	0.000000000000e+00	4.7123889
Ball 16	BALL_POWER	VSS	4.0000e-01	2.0000e+00	0.000000000000e+00	4.7123889
Ball 18	BALL_POWER	VSS	1.2000e+00	2.0000e+00	0.000000000000e+00	4.7123889
Ball 19	BALL_POWER	VSS	1.2000e+00	2.0000e+00	0.000000000000e+00	4.7123889
Ball 21	BALL_POWER	VSS	2.0000e+00	2.0000e+00	0.000000000000e+00	4.7123889
Ball 22	BALL_POWER	VSS	2.0000e+00	2.0000e+00	0.000000000000e+00	4.7123889

MCAD export migration to Parasolid enhancements

- Improvements to port radial extent in HFSS 3D export
- Enhancements to Q3D net classification and performance
- Support spheroidal/oblong and cylinder solderballs

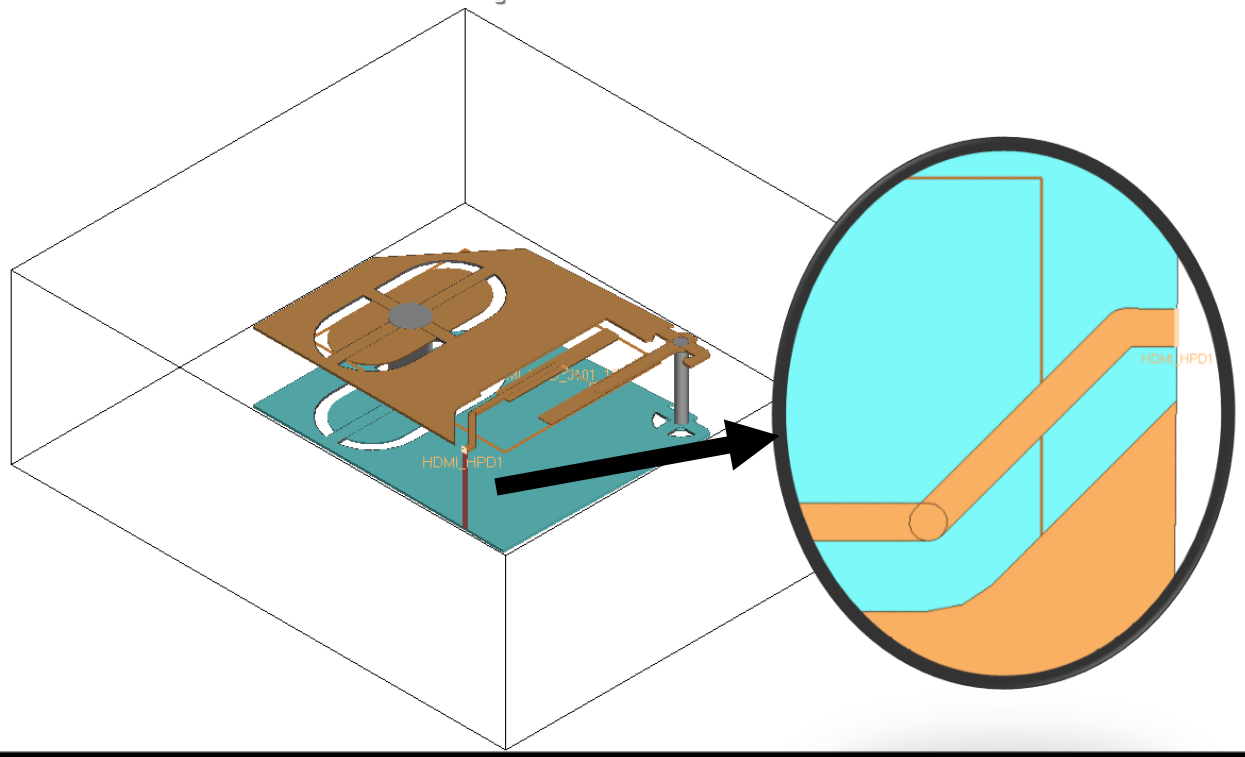




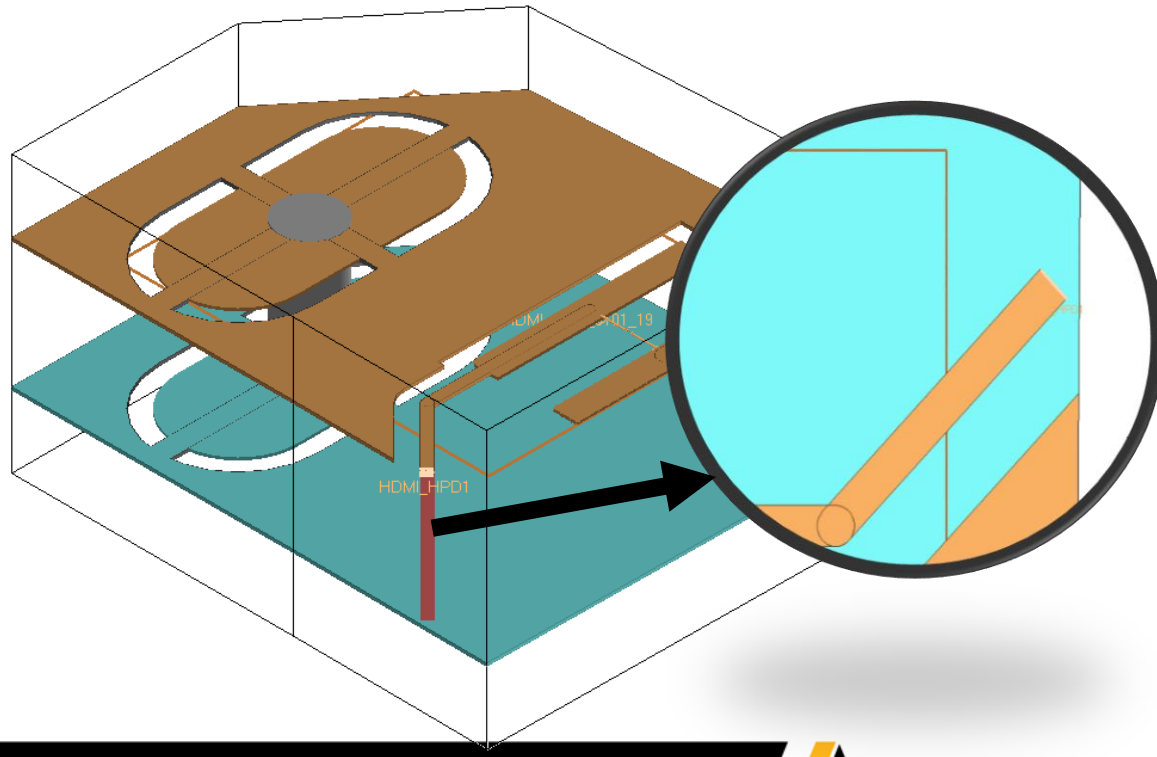
SIwave HFSS Region clipping and configuration enhancements [Beta]

- Provide an alternative way to generate HFSS regions in 3D Layout
  - Clip the dielectric to exact match the region outline and assign radiation boundary to exact match the region outline
  - Clip traces at region extents and recess the trace length by a factor of the trace width so the lumped ports are located inside the cutout (instead of been placed at the region boundary)

Current implementation

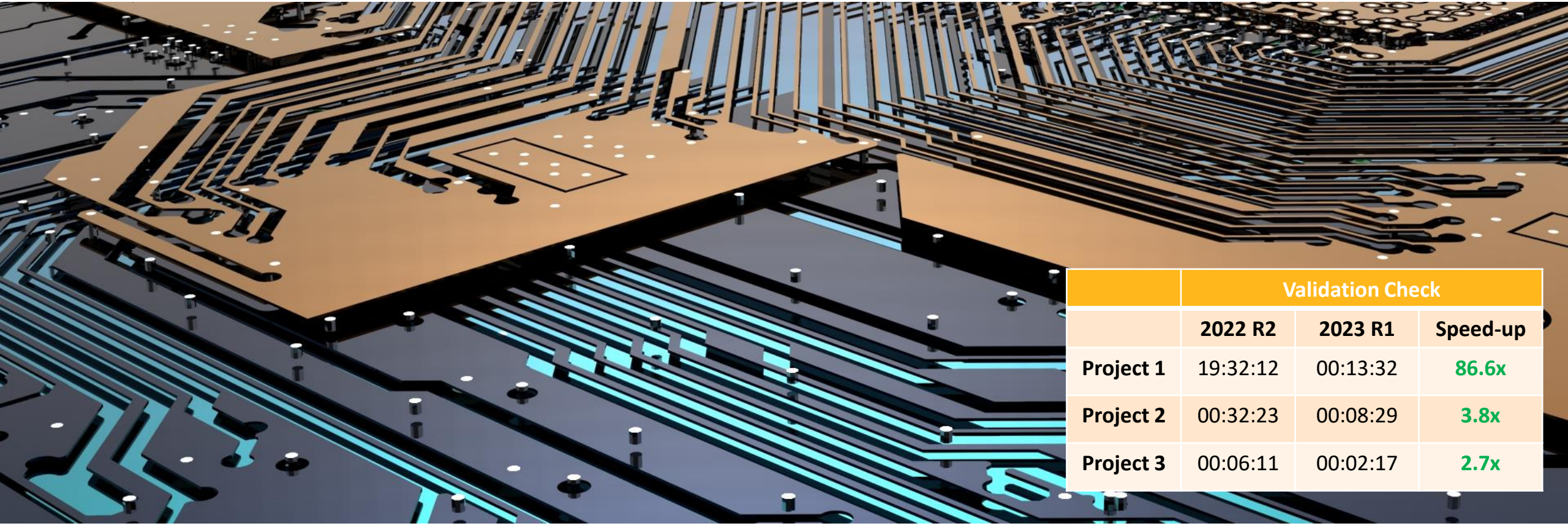


Conformal regions



Validation Check performance optimizations

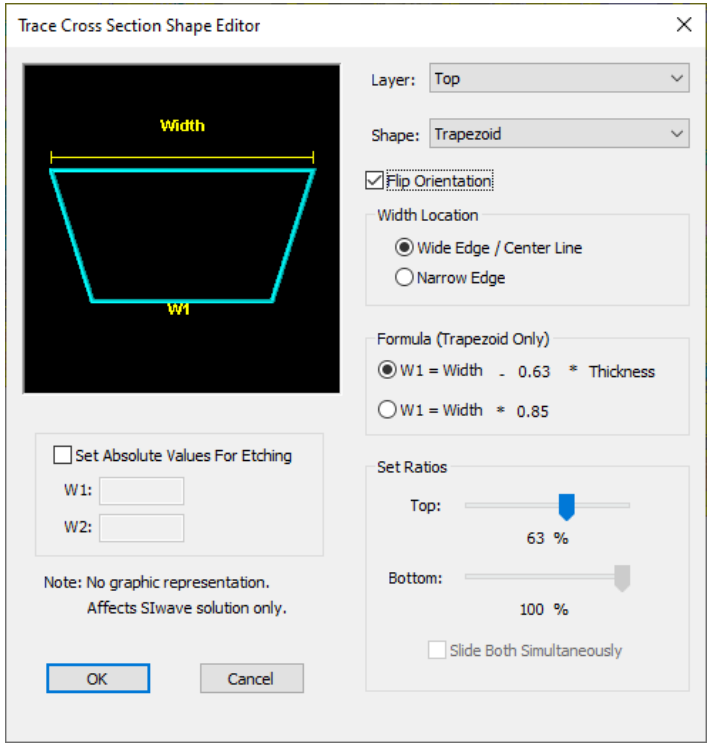
- Significant run time improvements compared to 2022 R2
- Performance improvements can be largely seen in designs containing large numbers of vias
  - Optimization to via-via overlapping algorithm



	Validation Check		
	2022 R2	**2023 R1**	**Speed-up**
Project 1	19:32:12	00:13:32	**86.6x**
Project 2	00:32:23	00:08:29	**3.8x**
Project 3	00:06:11	00:02:17	**2.7x**

SIwave miscellaneous enhancements

- Specify trace cross section orientation
  - Users can flip the orientation of cross sections
- SNA report and scripting
  - SNA now support scripting and it can be executed in non graphical mode
  - Export reports in HTML and CSV formats
- Handling of S-parameter components
  - Improve the robustness of simulation when using S-parameter models as components
  - Automatic verification of symmetry, DC extrapolations, etc...

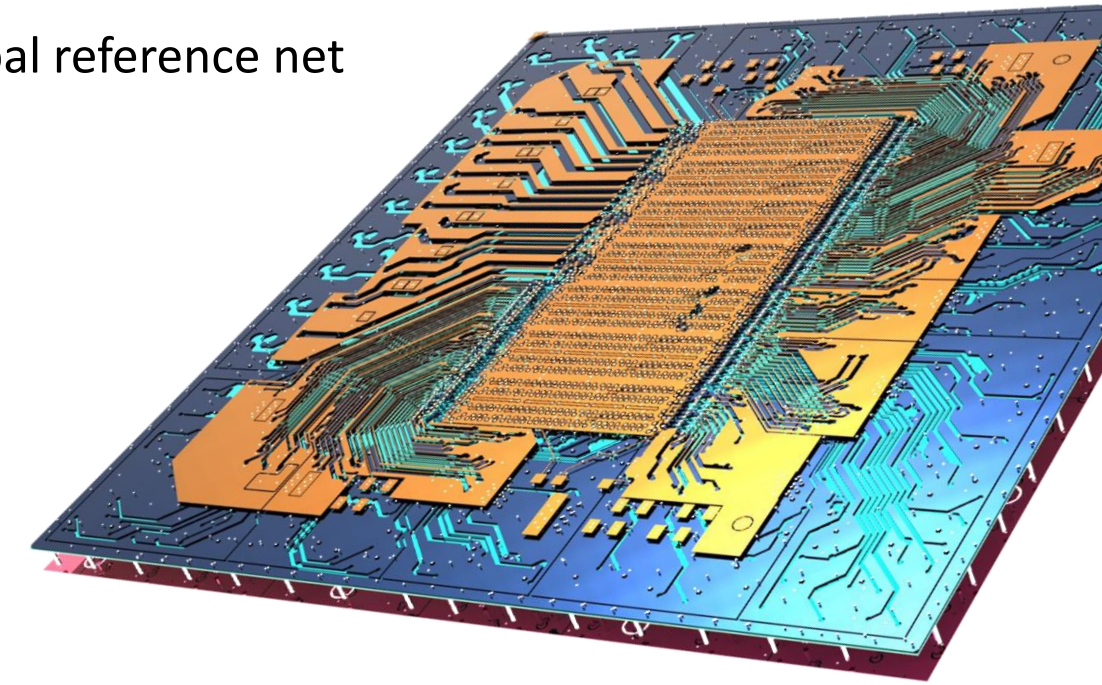


CPA 2023 R1

- Package netlist remapping to fit any arbitrary chip
  - Objective is to map an already extracted package netlist from CPA into the footprint of a new chip
  - Considering that the model has already been extracted using a PLOC file, this new capability remaps the results using a new PLOC file.

- Support multiple ground nets for VRMs
  - Until 2022 R2 CPA had a restriction of using a single global reference net

- Improvements to the robustness, reliability and repeatability of results improvements
  - Improve the robustness of error/exception handling in the solver code and providing informative messages to users



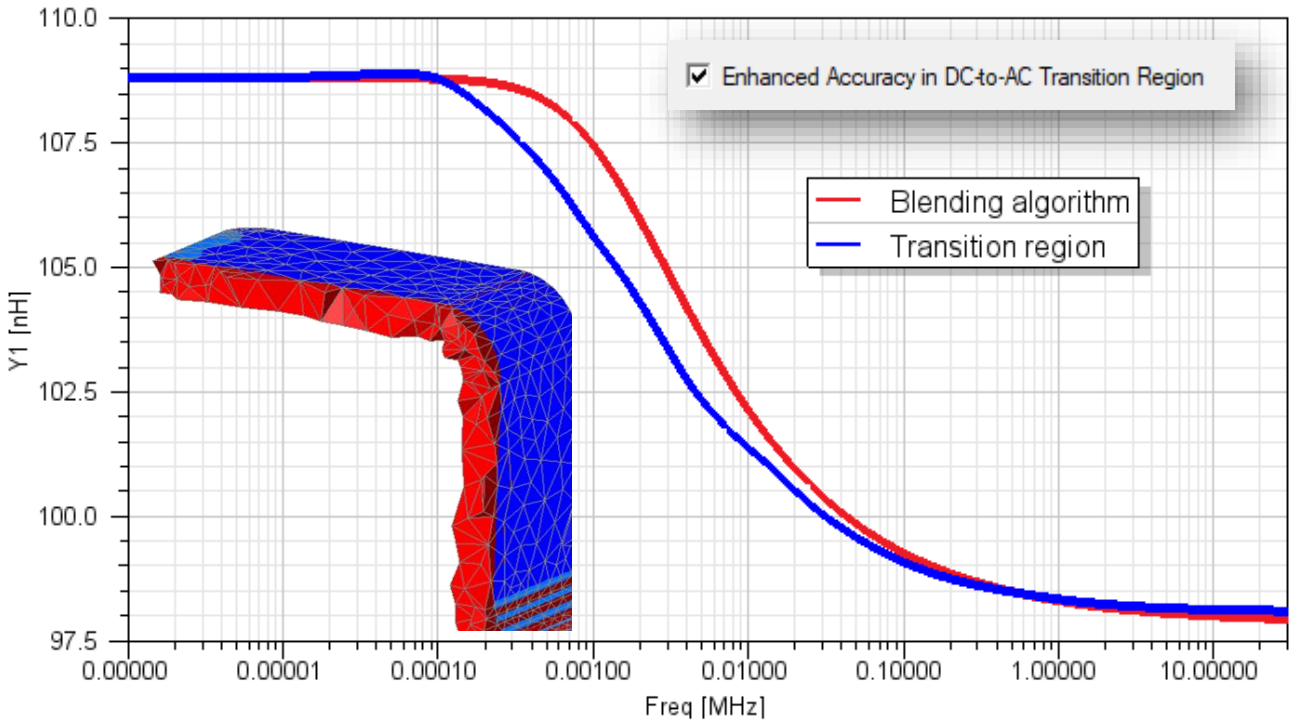
Q3D Extractor

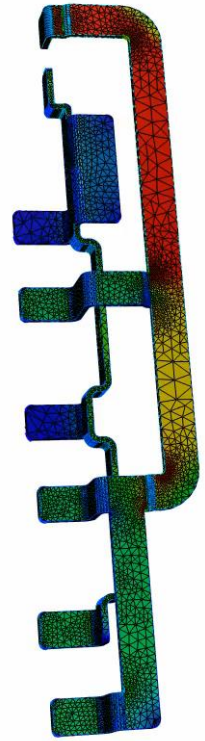
Ansys

DC to AC transition region RL analysis (Beta)

- New transition region solver to explicitly solve inside conductors at AC
- Improves results in the transition region for specific applications (power electronics)

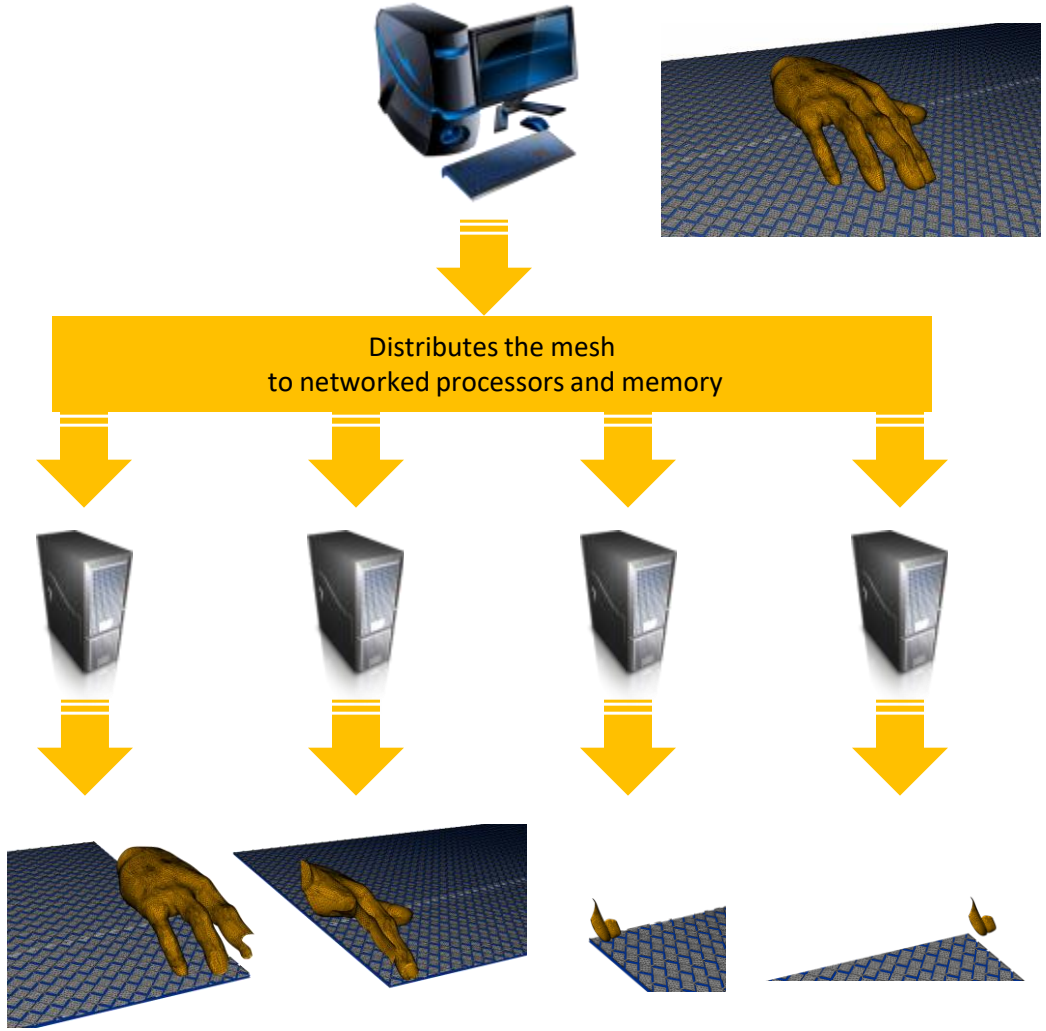
Busbar example





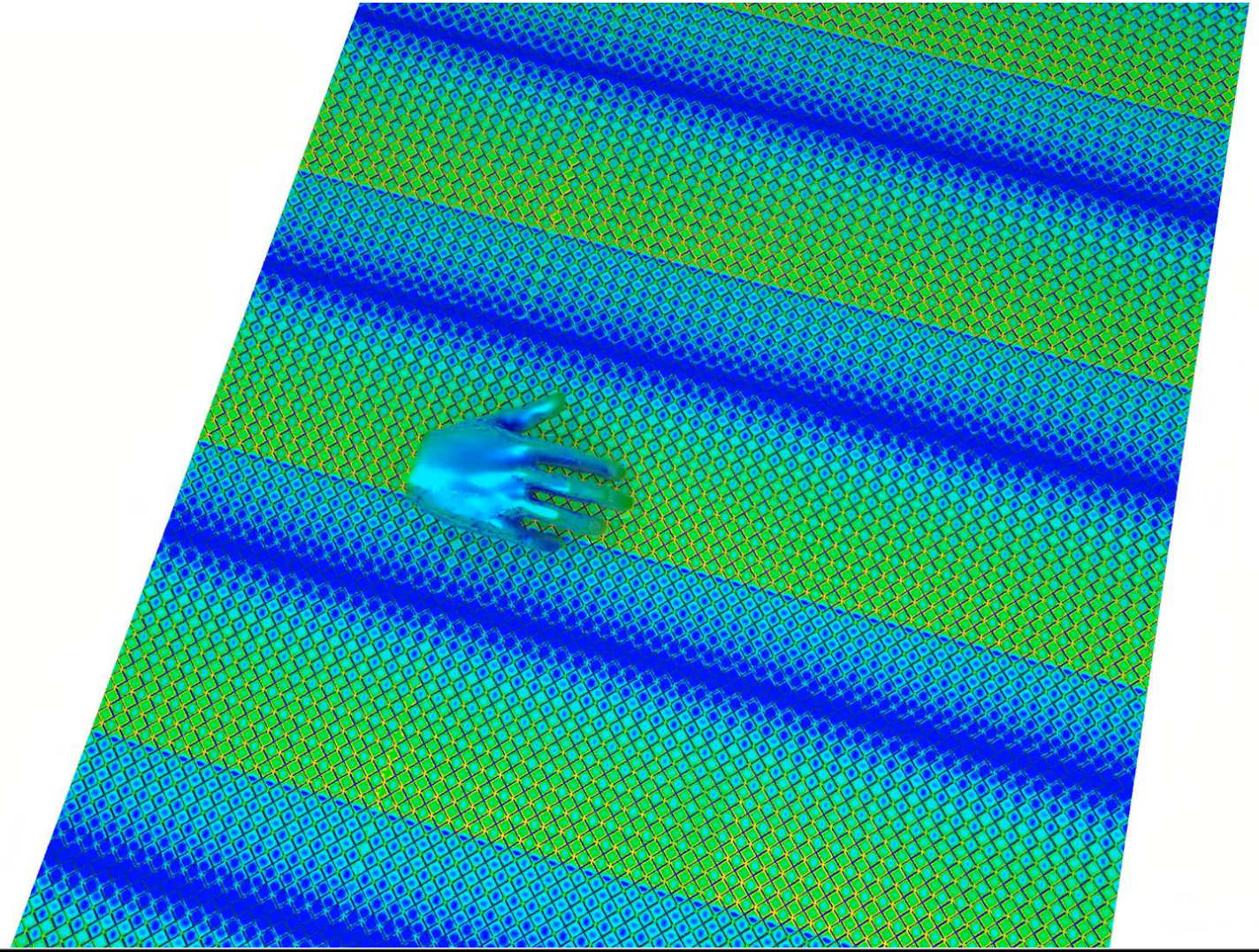
Distributed CG solver (Beta)

- In earlier versions the HPC on the CG solver supported only the distribution of the nets or frequencies.
- Large problems with a large mesh could run out of memory due to the limitation of RAM on a single machine
- In 2023 R1 version a distributed memory CG solver (MPI-FMM) has been developed in order to handle designs that require mesh sizes of hundreds of millions of elements.
- In this new solver we redistribute the mesh to the MPI-tasks available and as a result each task handles only a partial mesh.



Distributed CG solver (Beta)

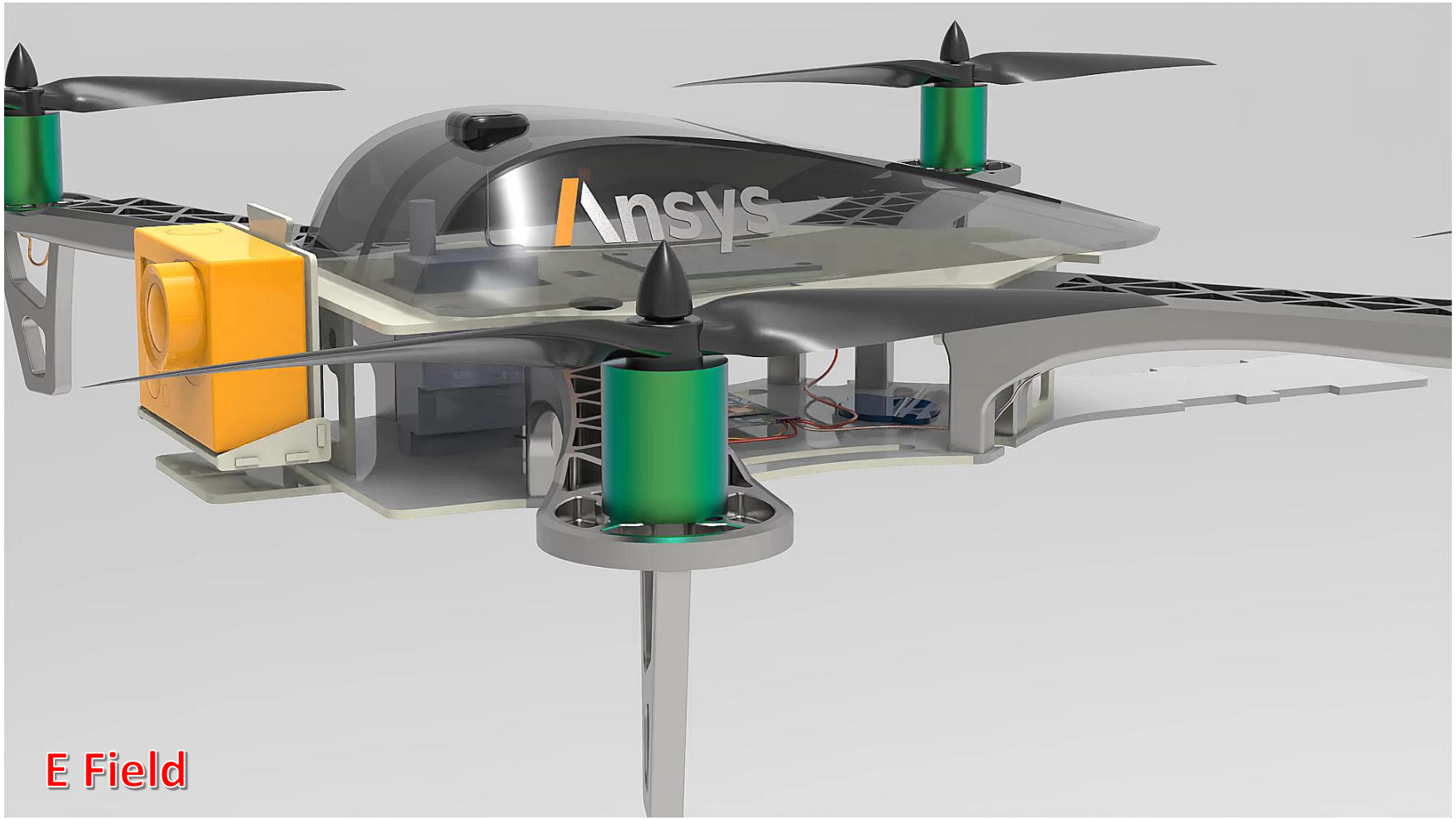
Large capacitive touchscreen example



Cores	Time	Speed-up
4	3:00:05	1.0
16	1:03:28	2.8
32	0:41:51	4.3
64	0:21:00	8.6
96	0:14:02	12.8

Electric and Magnetic field computation performance

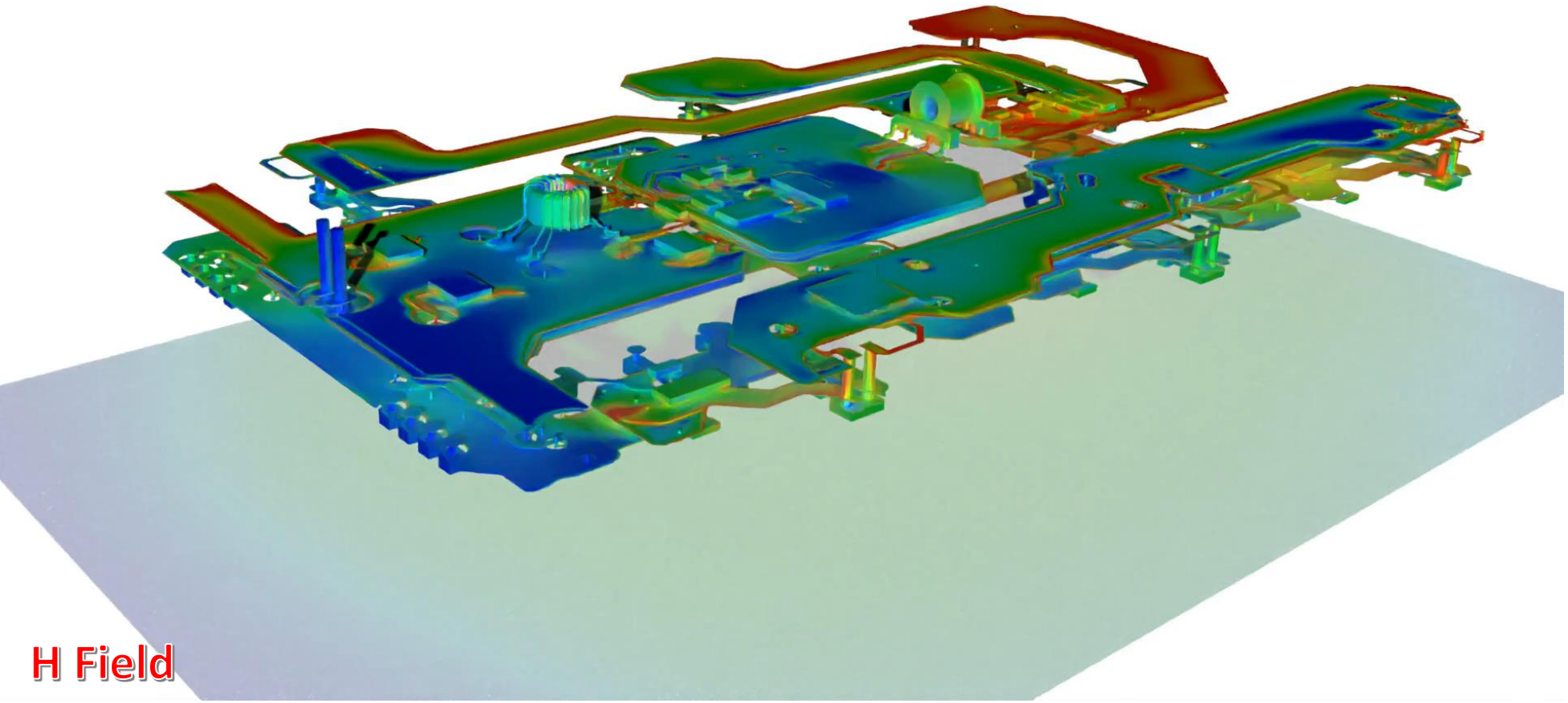
- New algorithm to compute E and H fields on the surface and on the volume



PCKG on PCB in a drone example

Version	Time
2022 R2	00:41:31
2023 R1	00:12:47

Electric and Magnetic field computation performance



H Field

PCB with components

Version	Time
2022 R2	00:18:35
2023 R1	00:00:47

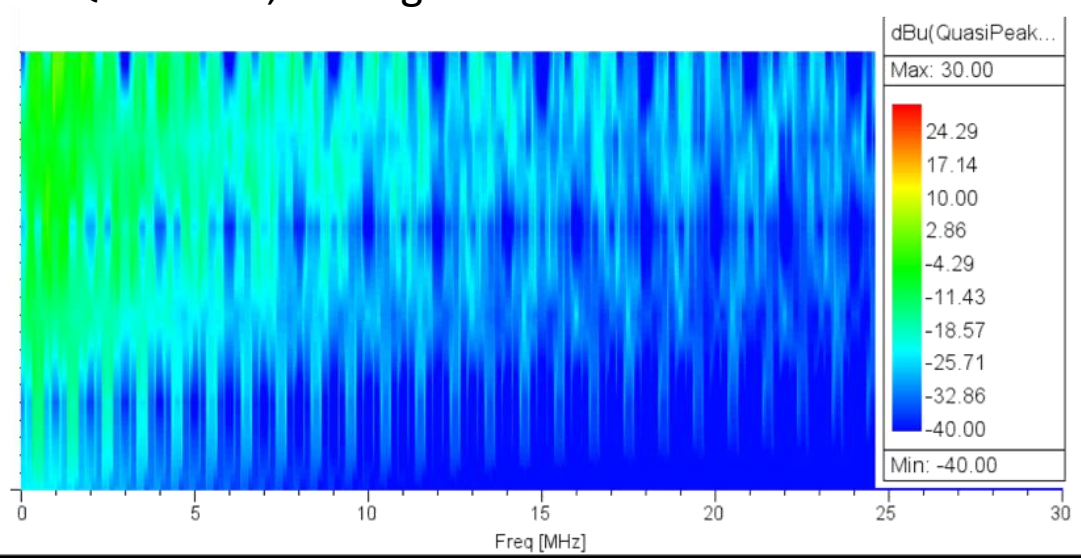
2023 R1 is 23.7x faster for this example

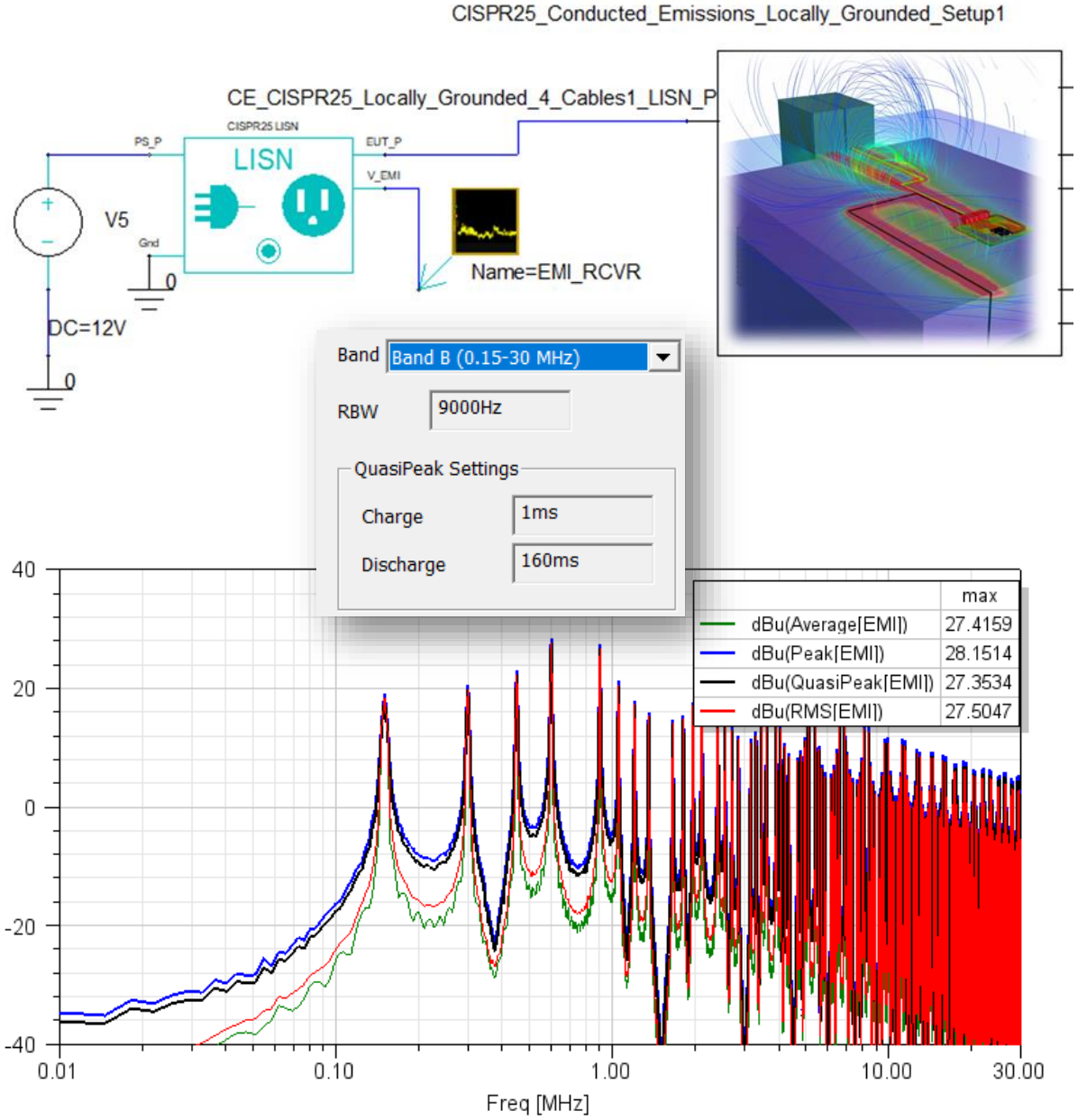
Circuits and SPISim

Ansys

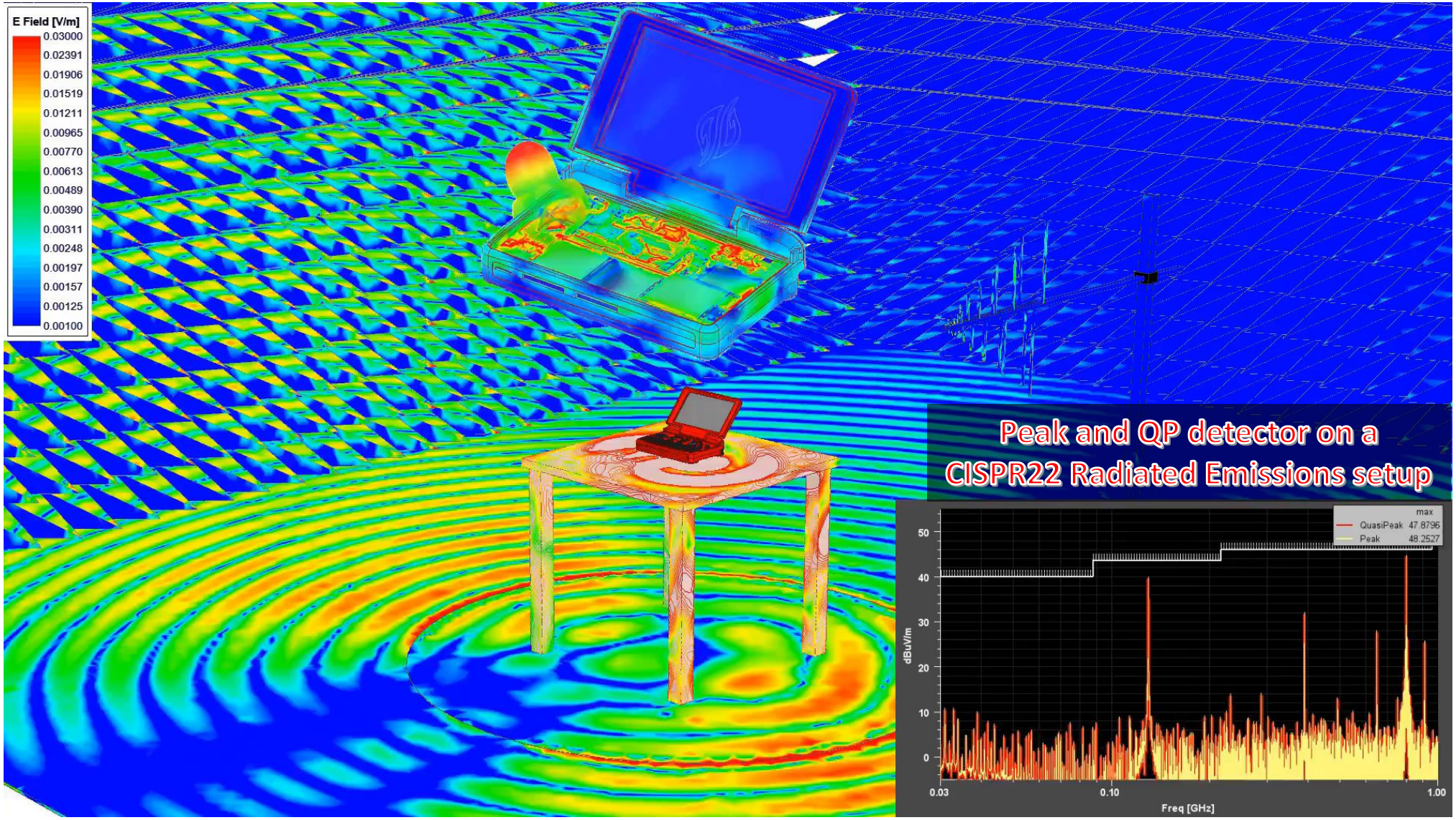
2023.1 – EMI Receiver [Beta]

- EMI Receiver
  - Transient signal undergoes a Short-Time-Fourier-Transform (STFT) analysis with Gaussian window and output a 3D spectrogram data which shows frequency component change in the signal with respect to time.
  - The Spectrogram data is passed through the desired EMI detectors to obtain the emissions in the selected frequency range.
  - Supports CISPR16-1-1 Band A to D with Peak, QuasiPeak, Average and RMS Detections.





2023.1 – EMI Receiver [Beta]

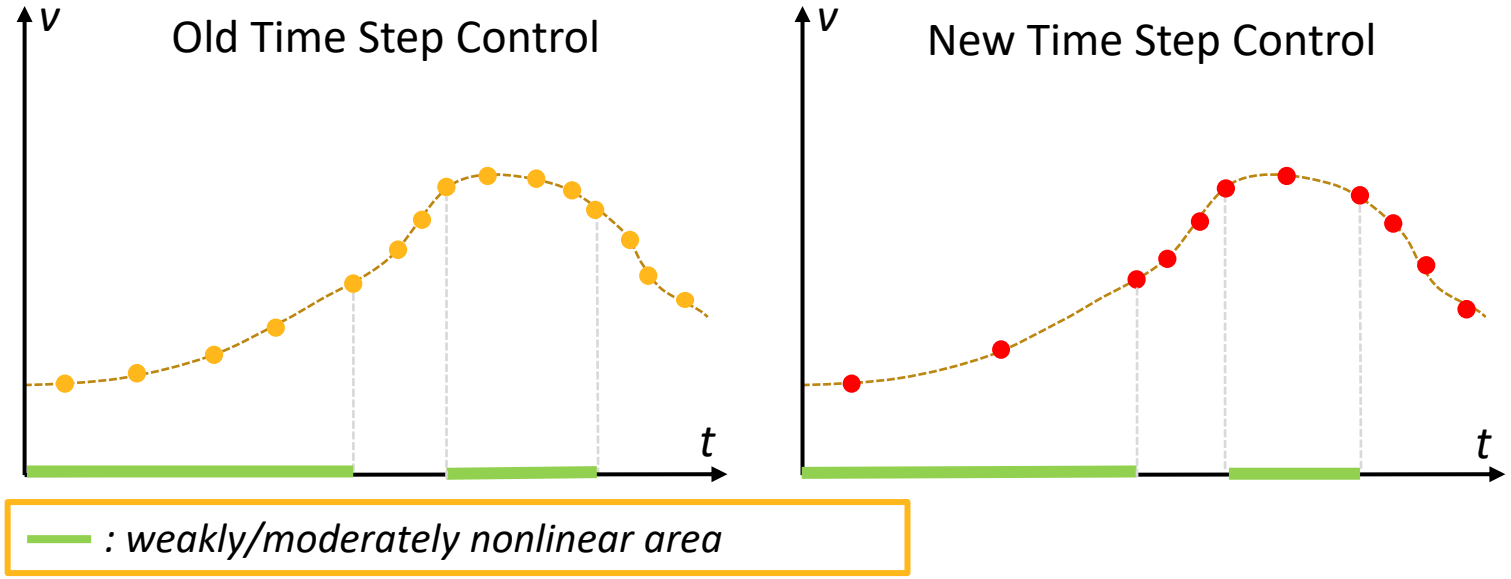


2023.1 – Adaptive time stepping improvements

Motivation:
- Small time step can improve the chance of convergence.
- Small time step slows down simulation.
- Would like a moderately large time step without loss of accuracy and convergency.

Solution:
- Use the number of Newton iterations as an indicator of nonlinearity.
- Keep the philosophy of the existing multi-stage time step control algorithm.
- Increase time step for weak/moderate nonlinearity.

Impact:
- Reduce the total number of time steps and Newton iterations.
- Improve simulation time.

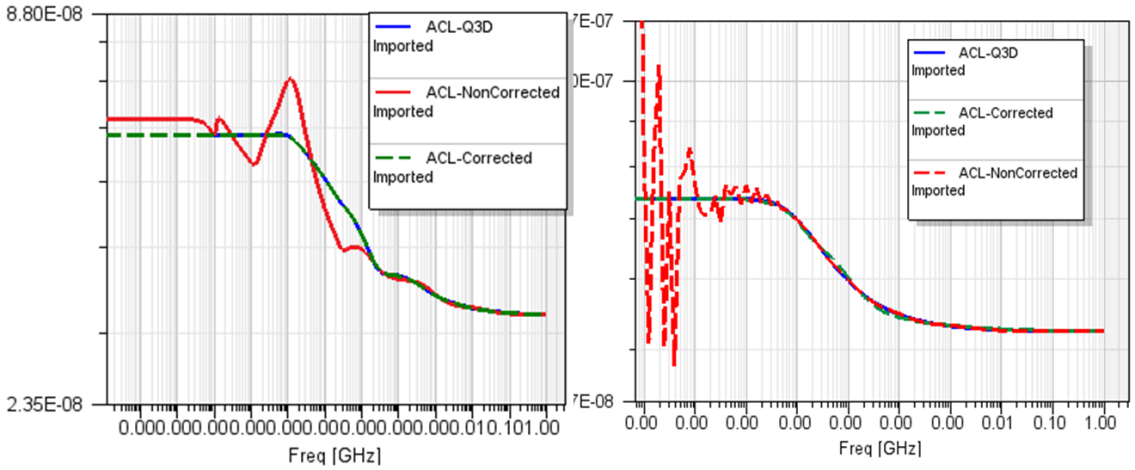


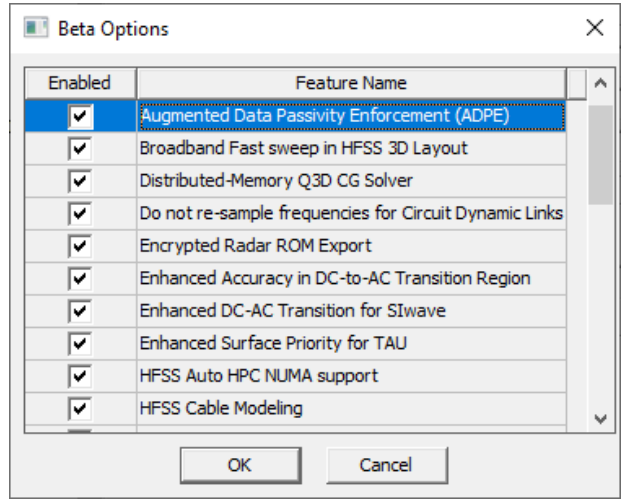
	Two-stage LTE Adaptivity			Two-stage LTE & nonlinearity Adaptivity			Impr. in Newton step (%)	Impr. in Sim. time (%)
h	# time step	Avg. Newton	cpu time(s)	# time step	Avg. Newton	cpu time(s)		
1e-9	9.90e+02	3.8	0.233	9.48e+02	3.9	0.223	4.24	4.29
1e-11	7.41e+04	2	7.18	6.69e+04	2	6.702	9.72	6.66
1e-13	7.39e+06	2	718.997	6.68e+06	2	658.687	9.61	8.39

State space fitting enhancements

- Improvements to Q3D RLGC Spice export
  - With the new AC-to-DC transitions region Q3D solver a new algorithm was developed to enforce stability and automatically perform causal correction.

- New Augmented Data Passivity Enforcement (ADPE) algorithm[Beta]
  - New state-space fitting option that helps with passivity enforcement when the S-data is under-sampled.
  - Improves the use of Tsuk-White Algorithm (TWA) interpolation and passivity enforcement where the set of basis points are usually under-sampled.





AMI Support for DDR5 asymmetric rising/falling edges

Motivation:

- AMI was originally developed for SerDes applications. The channel and the IBIS model driving it for the step response computation were assumed fully LTI. A single step (impulse) response characterized the entire channel.

Issue:

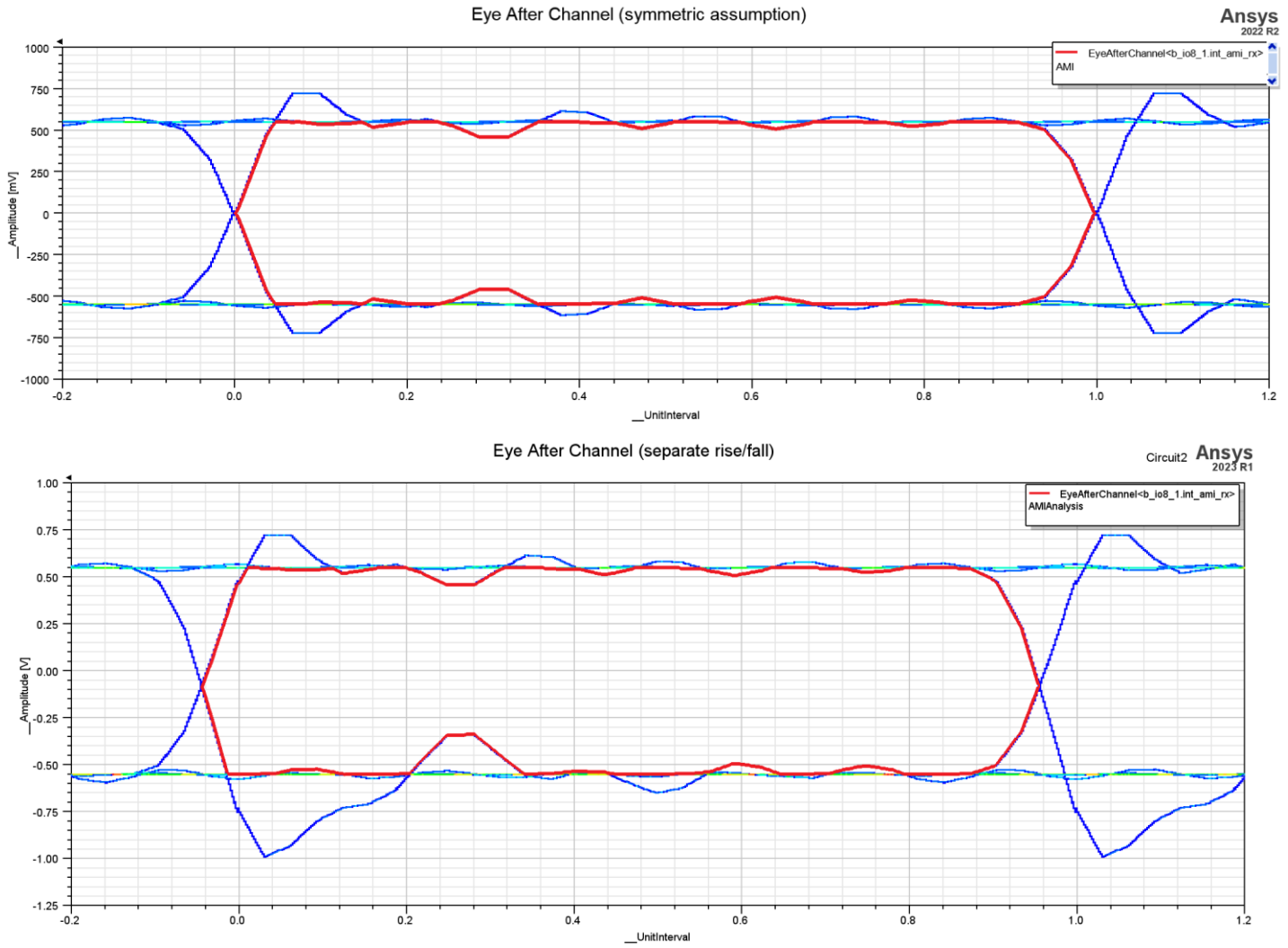
- AMI simulations are now used for DDR5 devices.
- DQ channels are single-ended. AMI model makers provide IBIS models that include one significant non-linearity, the rising and falling edges are significantly different.

Solution:

- For single-ended applications, AMI analysis no longer assumes a single step (impulse) response is sufficient.
- Channel output is based on convolving with different rising/falling responses.

Effect:

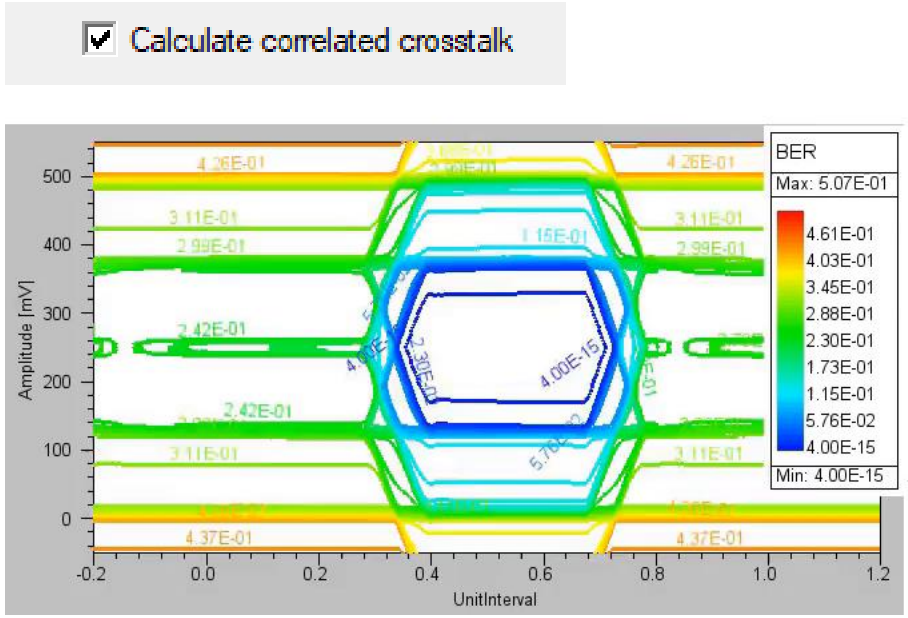
- Results will be correct for asymmetric signals (e.g., DDR5 DQ).

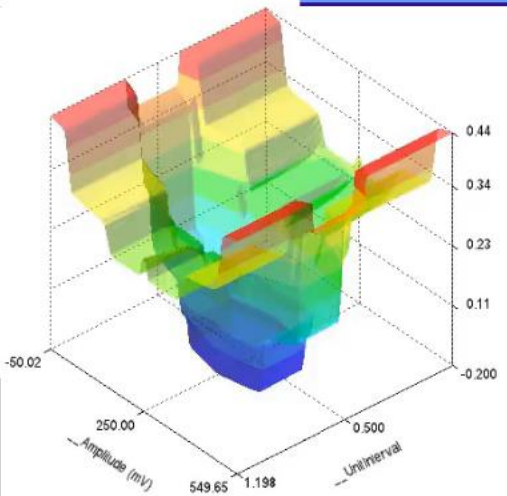


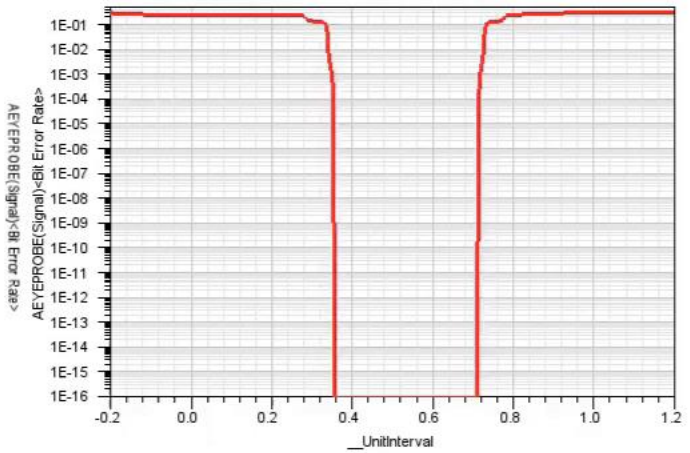
Correlated crosstalk option for VerifEye

- Correlated crosstalk preserves the delays (i.e. jitter) between victim and aggressor lanes
- Uncorrelated crosstalk simulates the effects of crosstalk energy that can occur anywhere in the victim's eye diagram with equal probability

Correlated crosstalk VerifEye analysis of two parallel traces







Calculate ERL w/o using COM flow

Motivation:

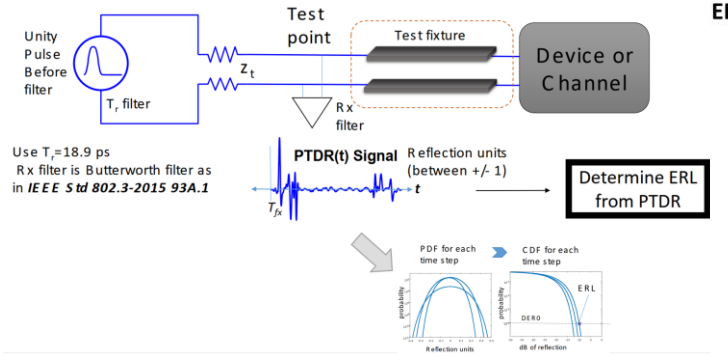
- SPISim's COM provides ERL calculation, but COM requires a config. settings which has 100+ input parameters.
- AEDT's user would like to calculate ERL directly without going through COM flow.

Solution:

- Flow has been refactored. An individual ERL menu item has been added in the SPro menu for direct access.
- NG batch mode and UDO/UDS based approaches have also been implemented to support direct ERL calculation.

Impact:

- AEDT user can import one or more .snp file(s) and calculate their ERL values in GUI or batch mode.
- HFSS 3D Layout/Circuit users now can optimize their design based on ERL results directly.



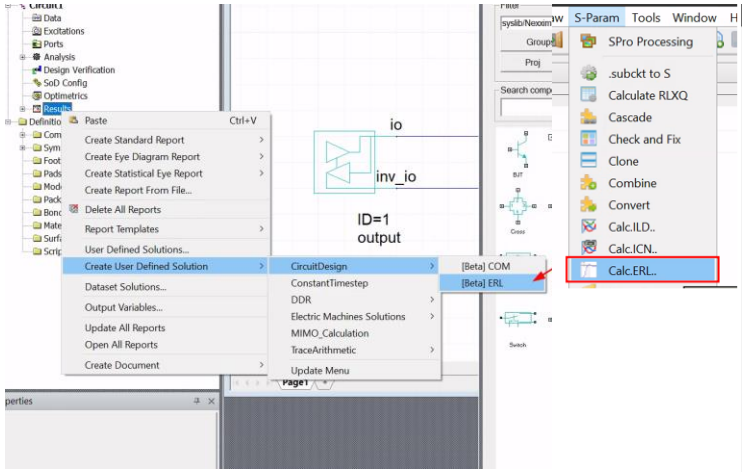
ERL: Effective Return Loss using PTDR

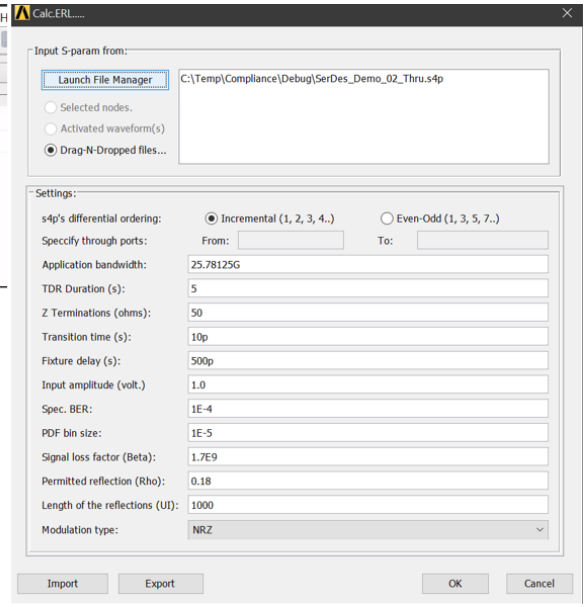
ERL Computation Parameters

- N_{bx} is the number for DFE taps or set by referencing clause
- T_b is the time for one symbol (aka UI) in ns
- t is time in ns
- T_{fx} is the time in ns associated with the end of the test fixture
- β_x is loss/ratio per unit time derived from the reference package loss in GHz
- ρ_x is the permitted reflection from the "missing side" of the channel
  - ρ_x is a reflection ratio and thus unitless

$$R_{eff}(t) = PTDR(t) \left(\rho_x (1 + \rho_x) e^{\frac{\left(\frac{t - T_{fx} - (N_{bx}+1)}{T_b}\right)^2}{(N_{bx}+1)^2}} \right) 10^{\frac{\beta_x \left(t - T_{fx} - T_b (N_{bx}+1)\right)}{20}}$$

DFE re-reflection compensation — Package Loss compensation





SPISim: New SERDES Compliance checks

Motivation:

- AEDT/HSFSS users would like to perform compliance check for some SERDES standards/specs.
- Some specs. have input data comprised of various sections, automatic “cascading” may be needed during process.

Solution:

- Enhanced SPISim’s compliance check to support eight more industry standards.
- Will “cascaded” .snp files automatically if needed for various aspect of compliance checking.
- Both SPISim GUI mode and NG batch (GUI or non-GUI) are supported.
- Also provide TDR report for additional design performance metrices report.

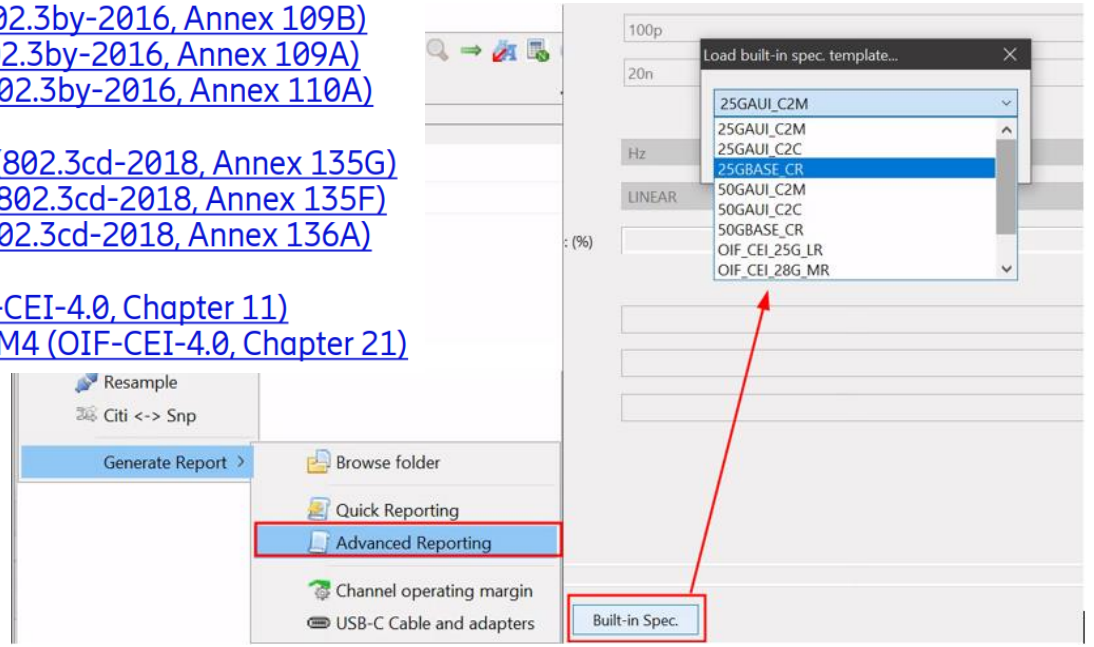
Impact:

- AEDT/HFSS users can now perform compliance checks for generated .snp files within the ANSYS environment/toolsets.

25GAUI C2M (802.3by-2016, Annex 109B)
25GAUI C2C (802.3by-2016, Annex 109A)
25GBASE-CR (802.3by-2016, Annex 110A)

50GAUI-1 C2M (802.3cd-2018, Annex 135G)
50GAUI-1 C2C (802.3cd-2018, Annex 135F)
50GBASE-CR (802.3cd-2018, Annex 136A)

CEI-25-LR (OIF-CEI-4.0, Chapter 11)
CEI-56G-LR-PAM4 (OIF-CEI-4.0, Chapter 21)



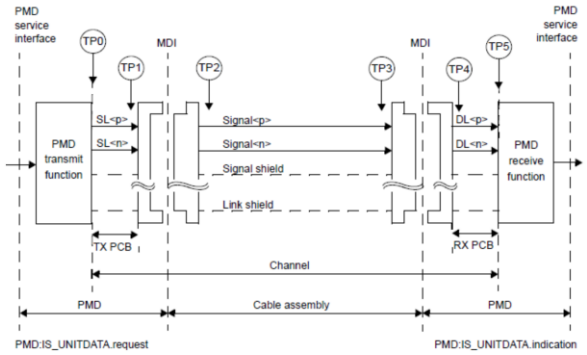
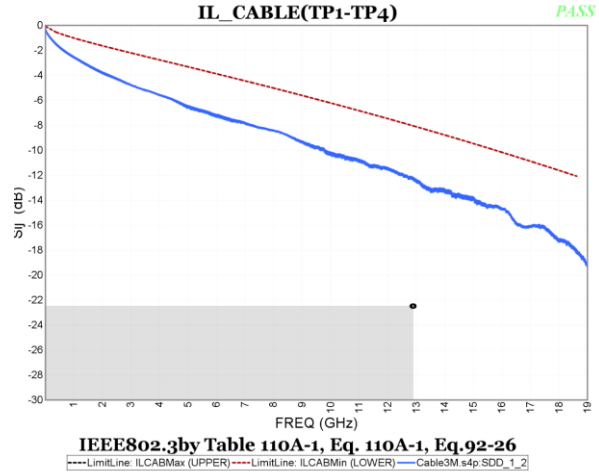


Figure 110–2—25GBASE-CR or 25GBASE-CR-S link (one direction is illustrated)



AEDT Desktop and Core

Ansys

Ansys Electronics Desktop

- Parasolid kernel for 3D Modeler
  - Official migration to Parasolid modeling kernel
- Auto multi-level distribution for LSDSO
  - Each ansysedt process is free to automatically determine how to best utilize allocated available cores (solver distribution, frequency distribution, etc…)
- Native non-graphical image export
  - ExportModelImageToFile script command works in graphical and -ng mode on both Windows & Linux
- Enhancements to object-oriented property scripting
  - Additional scripts to handle datasets and retrieve information


Ansys